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MS-7696 Ver:1.0

CPU:

AMD FM1

System Chipset:

AMD - Hudson D3

On Board Chipset:

LPC Super I/O --F71869A

LAN-Realtek 8111E

Azalia CODEC - Realtek ALC892/887

Main Memory:

DDR III * 4 (max 32G)

Expansion Slots:

PCI Express X16 Slot * 2

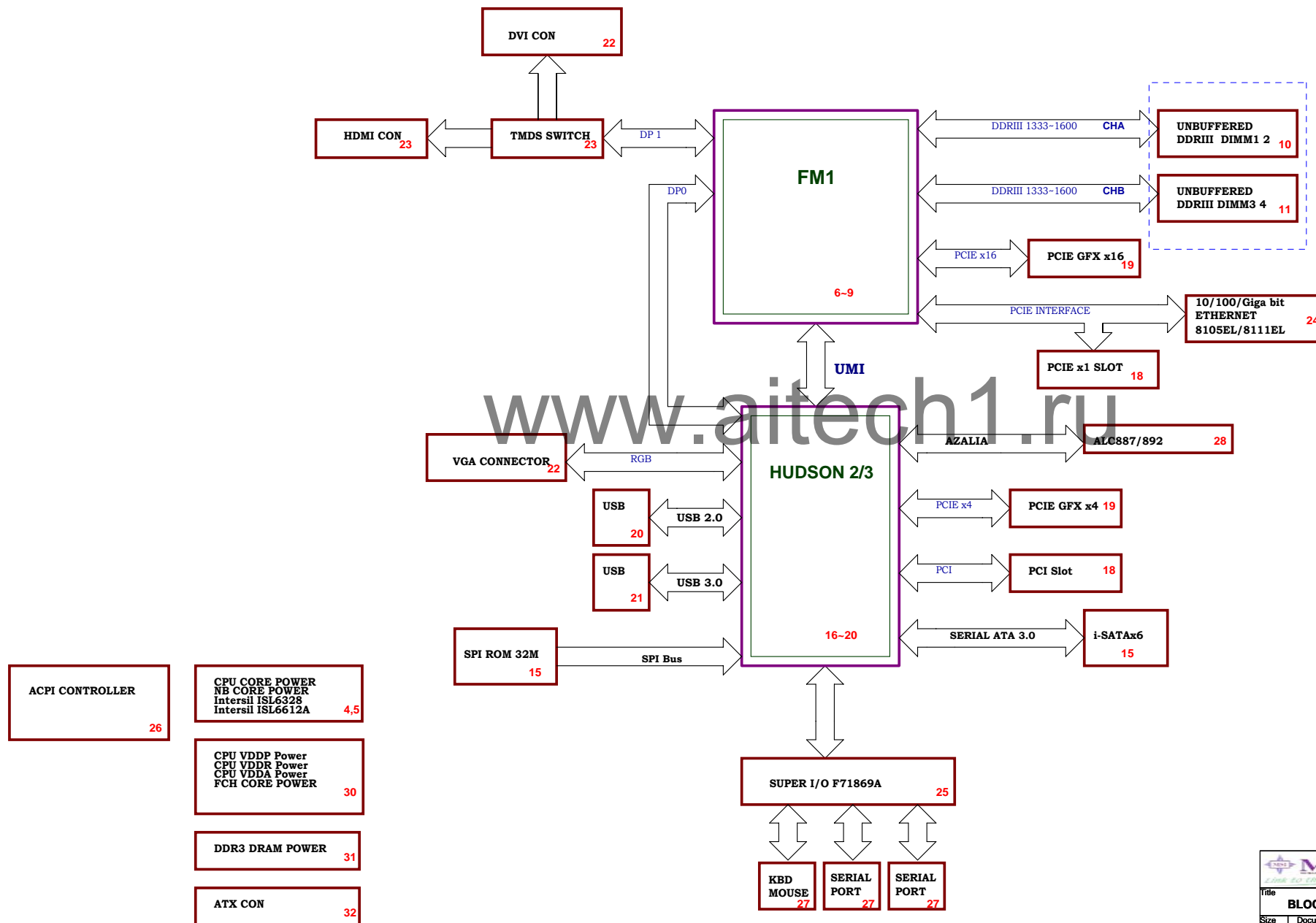
PCI Express X1 Slot * 1

PCI Slot * 1

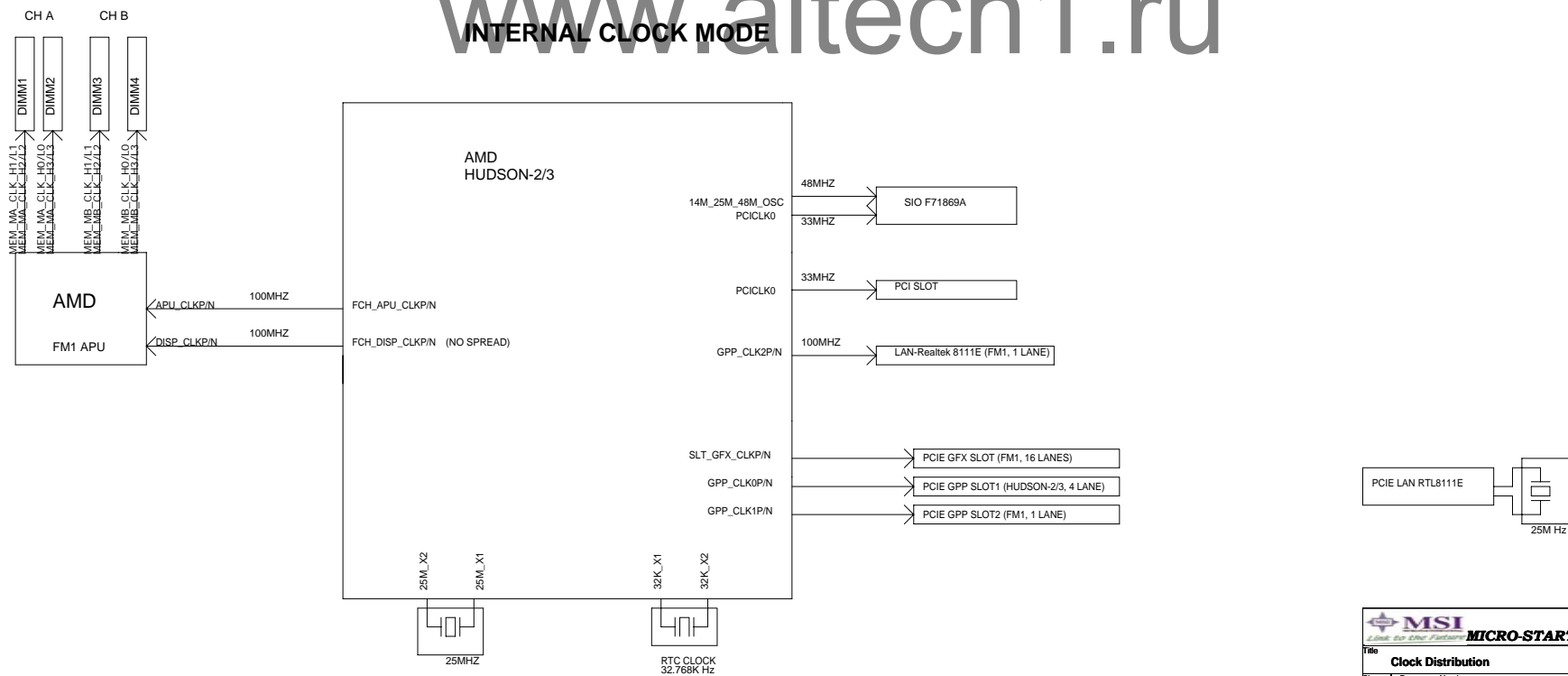
VRM

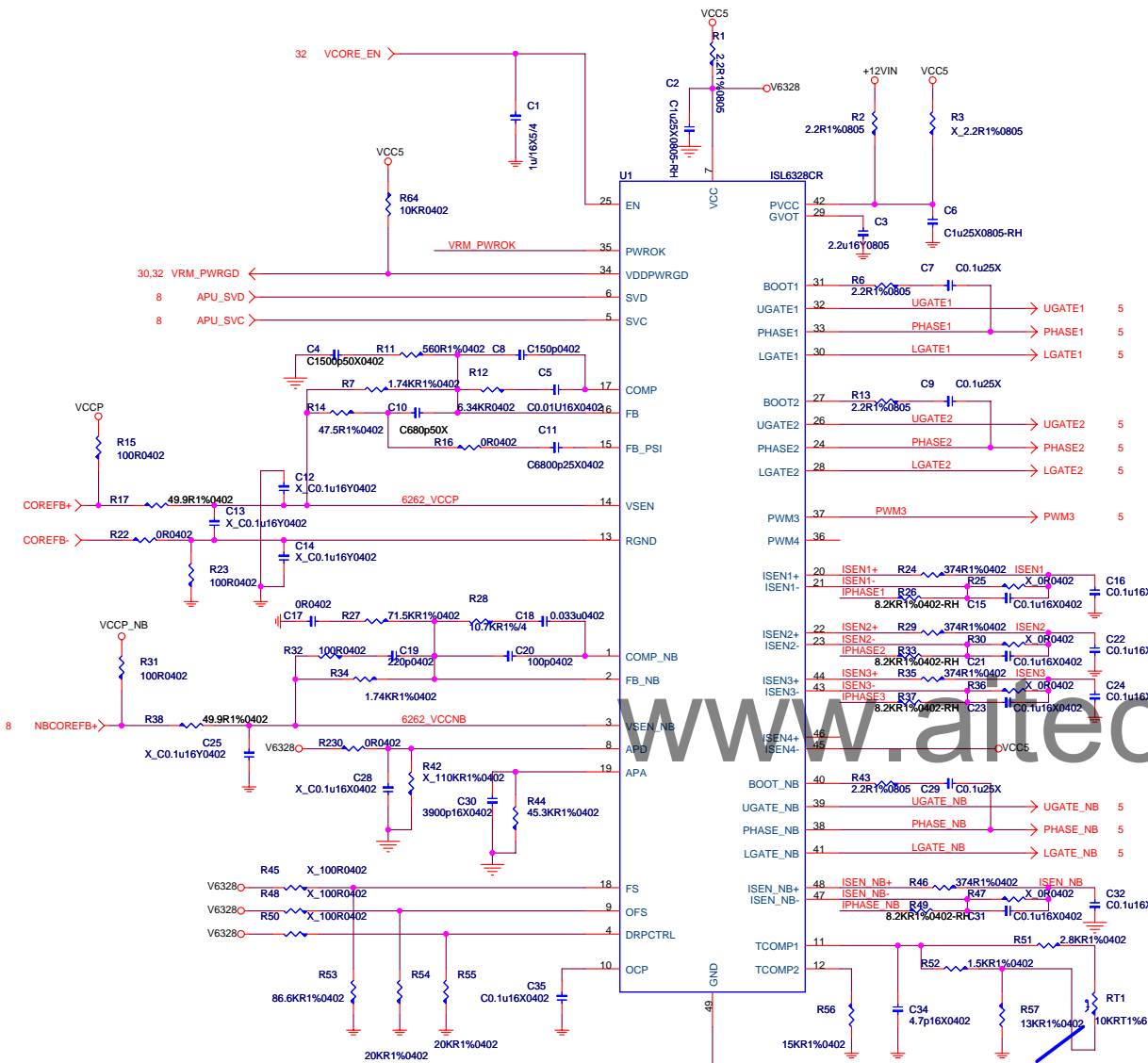
Controller - Intersil ISL6328 3+1 Phase

FUSION BLOCK DIAGRAM



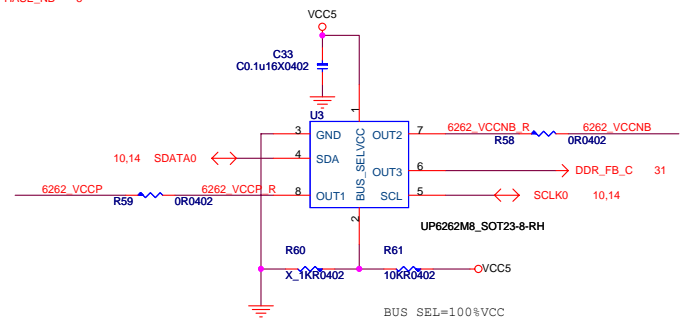
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BOTTOM PAD
CONNECT TO GND
Through 8 VIAS

Close PHASE1 Output Choke Vcore side

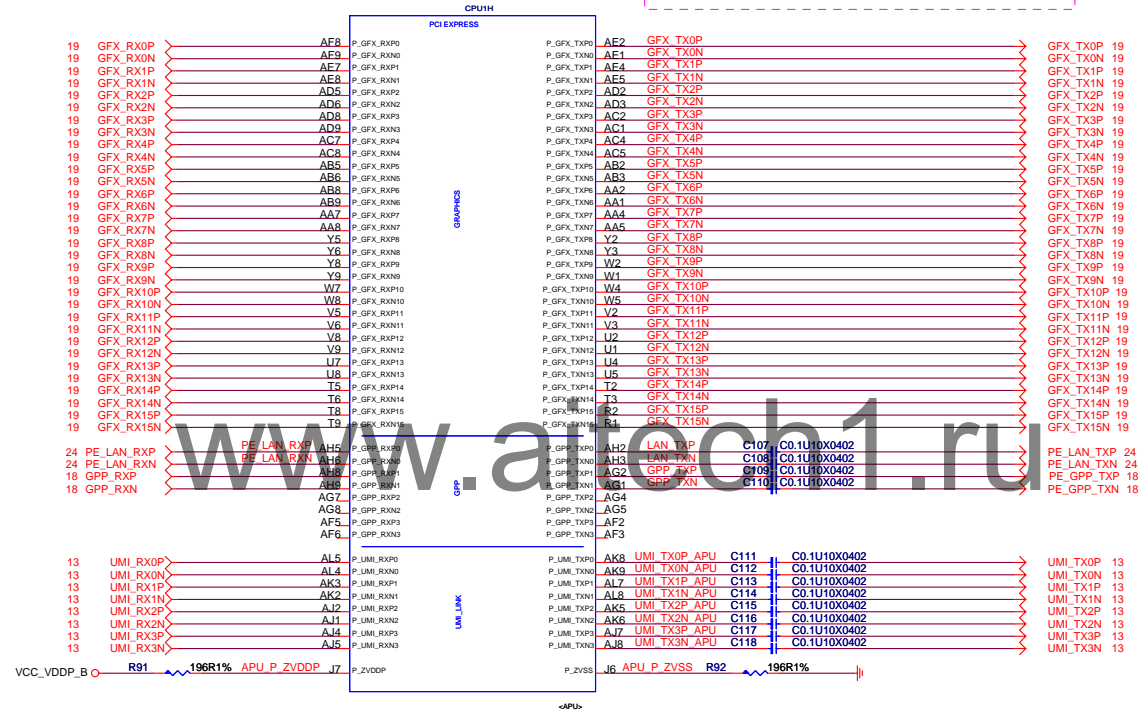


I2C address:0X20

MICRO-START INT'L CO.,LTD.		
Title		
Intersil ISL6328 3+1 Phase		
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FM1 PCIE I/F

mach@CRB PCIE AC Capacitors:75nF to 200nF
Layout: PLACE CAPS WITH APU < 1 INCH
ROUTE ALL PCIE AS 85OHM +/-10%



FM1DDR3 IF

10 MEM_MA_DQS_L[7..0] <--

10 MEM_MA_DQS_H[7..0] <--

10 MEM_MA_DM[7..0] <--

10 MEM_MA_ADD[15..0] <--

10 MEM_MA_BANK0 <--

10 MEM_MA_BANK1 <--

10 MEM_MA_BANK2 <--

MEM MA DM0 H12
MEM MA DM1 E17
MEM MA DM2 H21
MEM MA DM3 F25
MEM MA DM4 AF29
MEM MA DM5 AE25
MEM MA DM6 AG21
MEM MA DM7 AF17
MEM MA DM8 G29

MEM MA DOS H0 G13
MEM MA DOS L0 F13
MEM MA DOS H1 H17
MEM MA DOS L1 G17
MEM MA DOS H2 F21
MEM MA DOS L2 E21
MEM MA DOS H3 G26
MEM MA DOS L3 G25
MEM MA DOS H4 AE28
MEM MA DOS L4 AE29
MEM MA DOS H5 AG25
MEM MA DOS L5 AG25
MEM MA DOS H6 AF20
MEM MA DOS L6 AF21
MEM MA DOS H7 AE16
MEM MA DOS L7 AD16

MEM MA CLK H0 U27
MEM MA CLK L0 U26
MEM MA CLK H1 T23
MEM MA CLK L1 U23
MEM MA CLK H2 T25
MEM MA CLK L2 T26
MEM MA CLK H3 R27
MEM MA CLK L3 R28

10 MEM_MA_CKE0 <--

10 MEM_MA_CKE1 <--

10 MEM_MA0_ODT0 <--

10 MEM_MA0_ODT1 <--

10 MEM_MA1_ODT0 <--

10 MEM_MA1_ODT1 <--

10 MEM_MA0_CS_L0 <--

10 MEM_MA0_CS_L1 <--

10 MEM_MA1_CS_L0 <--

10 MEM_MA1_CS_L1 <--

10 MEM_MA_RAS_L <--

10 MEM_MA_CAS_L <--

10 MEM_MA_WE_L <--

10 MEM_MA_RESET# <--

10 MEM_MA_HOT# <--

APU_M_VREF <--

VCC_DDR <--

mach@CLOCK assignment can be changed

Layout:
Place within 1.5" of APU



Layout:
Place within 1.5" of APU

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MEM_MA_DATA[63..0] 10

11 MEM_MB_DQS_L[7..0] <--

11 MEM_MB_DQS_H[7..0] <--

11 MEM_MB_DM[7..0] <--

11 MEM_MB_ADD[15..0] <--

11 MEM_MB_BANK0 <--

11 MEM_MB_BANK1 <--

11 MEM_MB_BANK2 <--

MEM MB DM0 B12
MEM MB DM1 D16
MEM MB DM2 B20
MEM MB DM3 A25
MEM MB DM4 AL29
MEM MB DM5 AH25
MEM MB DM6 AK21
MEM MB DM7 A117
MEM MB DM8 D29

MEM MB DOS H0 D13
MEM MB DOS L0 C13
MEM MB DOS H1 A17
MEM MB DOS L1 B17
MEM MB DOS H2 B21
MEM MB DOS L2 C21
MEM MB DOS H3 D25
MEM MB DOS L3 C25
MEM MB DOS H4 AJ29
MEM MB DOS L4 AH29
MEM MB DOS H5 AK25
MEM MB DOS L5 AL25
MEM MB DOS H6 AJ20
MEM MB DOS L6 AJ21
MEM MB DOS H7 AL16
MEM MB DOS L7 AL17

MEM MB CLK H0 U30
MEM MB CLK L0 U29
MEM MB CLK H1 T29
MEM MB CLK L1 T28
MEM MB CLK L2 R31
MEM MB CLK L3 R30

11 MEM_MB_CKE0 <--

11 MEM_MB_CKE1 <--

11 MEM_MB0_ODT0 <--

11 MEM_MB0_ODT1 <--

11 MEM_MB1_ODT0 <--

11 MEM_MB1_ODT1 <--

11 MEM_MB0_CS_L0 <--

11 MEM_MB0_CS_L1 <--

11 MEM_MB1_CS_L0 <--

11 MEM_MB1_CS_L1 <--

11 MEM_MB_RAS_L <--

11 MEM_MB_CAS_L <--

11 MEM_MB_WE_L <--

11 MEM_MB_RESET# <--

11 MEM_MB_HOT# <--

MEM MB CKE0 J30

MEM MB CKE1 J28

MEM MB0_ODT0 AA30

MEM MB0_ODT1 AC30

MEM MB1_ODT0 AA31

MEM MB1_ODT1 AC29

MEM MB0_CS_L0 Y29

MEM MB0_CS_L1 AB29

MEM MB1_CS_L0 Y30

MEM MB1_CS_L1 AB31

MEM MB RAS_L W28

MEM MB CAS_L AA27

MEM MB WE_L AA28

MEM MB RESET# J27

MEM MB HOT# V28

MEM_MB_DATA[63..0] 11

MEM MB ADD0 V31
MEM MB ADD1 N28
MEM MB ADD2 P29
MEM MB ADD3 N29
MEM MB ADD4 N31
MEM MB ADD5 M30
MEM MB ADD6 M31
MEM MB ADD7 M28
MEM MB ADD8 M27
MEM MB ADD9 L30
MEM MB ADD10 W31
MEM MB ADD11 L29
MEM MB ADD12 K28
MEM MB ADD13 AG28
MEM MB ADD14 K31
MEM MB ADD15 J31

MEM MB BANK0 W29
MEM MB BANK1 V30
MEM MB BANK2 K29

MEM MB DM0 B12
MEM MB DM1 D16
MEM MB DM2 B20
MEM MB DM3 A25
MEM MB DM4 AL29
MEM MB DM5 AH25
MEM MB DM6 AK21
MEM MB DM7 A117
MEM MB DM8 D29

MEM MB DOS H0 D13
MEM MB DOS L0 C13
MEM MB DOS H1 A17
MEM MB DOS L1 B17
MEM MB DOS H2 B21
MEM MB DOS L2 C21
MEM MB DOS H3 D25
MEM MB DOS L3 C25
MEM MB DOS H4 AJ29
MEM MB DOS L4 AH29
MEM MB DOS H5 AK25
MEM MB DOS L5 AL25
MEM MB DOS H6 AJ20
MEM MB DOS L6 AJ21
MEM MB DOS H7 AL16
MEM MB DOS L7 AL17

MEM MB CLK H0 U30
MEM MB CLK L0 U29
MEM MB CLK H1 T29
MEM MB CLK L1 T28
MEM MB CLK L2 R31
MEM MB CLK L3 R30

MEM MB CKE0 J30

MEM MB CKE1 J28

MEM MB0_ODT0 AA30

MEM MB0_ODT1 AC30

MEM MB1_ODT0 AA31

MEM MB1_ODT1 AC29

MEM MB0_CS_L0 Y29

MEM MB0_CS_L1 AB29

MEM MB1_CS_L0 Y30

MEM MB1_CS_L1 AB31

MEM MB RAS_L W28

MEM MB CAS_L AA27

MEM MB WE_L AA28

MEM MB RESET# J27

MEM MB HOT# V28

MEM_MB_DATA[63..0] 11

MEM MB ADD0 V31
MEM MB ADD1 N28
MEM MB ADD2 P29
MEM MB ADD3 N29
MEM MB ADD4 N31
MEM MB ADD5 M30
MEM MB ADD6 M31
MEM MB ADD7 M28
MEM MB ADD8 M27
MEM MB ADD9 L30
MEM MB ADD10 W31
MEM MB ADD11 L29
MEM MB ADD12 K28
MEM MB ADD13 AG28
MEM MB ADD14 K31
MEM MB ADD15 J31

MEM MB BANK0 W29
MEM MB BANK1 V30
MEM MB BANK2 K29

MEM MB DM0 B12
MEM MB DM1 D16
MEM MB DM2 B20
MEM MB DM3 A25
MEM MB DM4 AL29
MEM MB DM5 AH25
MEM MB DM6 AK21
MEM MB DM7 A117
MEM MB DM8 D29

MEM MB DOS H0 D13
MEM MB DOS L0 C13
MEM MB DOS H1 A17
MEM MB DOS L1 B17
MEM MB DOS H2 B21
MEM MB DOS L2 C21
MEM MB DOS H3 D25
MEM MB DOS L3 C25
MEM MB DOS H4 AJ29
MEM MB DOS L4 AH29
MEM MB DOS H5 AK25
MEM MB DOS L5 AL25
MEM MB DOS H6 AJ20
MEM MB DOS L6 AJ21
MEM MB DOS H7 AL16
MEM MB DOS L7 AL17

MEM MB CLK H0 U30
MEM MB CLK L0 U29
MEM MB CLK H1 T29
MEM MB CLK L1 T28
MEM MB CLK L2 R31
MEM MB CLK L3 R30

MEM MB CKE0 J30

MEM MB CKE1 J28

MEM MB0_ODT0 AA30

MEM MB0_ODT1 AC30

MEM MB1_ODT0 AA31

MEM MB1_ODT1 AC29

MEM MB0_CS_L0 Y29

MEM MB0_CS_L1 AB29

MEM MB1_CS_L0 Y30

MEM MB1_CS_L1 AB31

MEM MB RAS_L W28

MEM MB CAS_L AA27

MEM MB WE_L AA28

MEM MB RESET# J27

MEM MB HOT# V28

MEM_MB_DATA[63..0] 11

MEM MB ADD0 V31
MEM MB ADD1 N28
MEM MB ADD2 P29
MEM MB ADD3 N29
MEM MB ADD4 N31
MEM MB ADD5 M30
MEM MB ADD6 M31
MEM MB ADD7 M28
MEM MB ADD8 M27
MEM MB ADD9 L30
MEM MB ADD10 W31
MEM MB ADD11 L29
MEM MB ADD12 K28
MEM MB ADD13 AG28
MEM MB ADD14 K31
MEM MB ADD15 J31

MEM MB BANK0 W29
MEM MB BANK1 V30
MEM MB BANK2 K29

MEM MB DM0 B12
MEM MB DM1 D16
MEM MB DM2 B20
MEM MB DM3 A25
MEM MB DM4 AL29
MEM MB DM5 AH25
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MEM MB DM7 A117
MEM MB DM8 D29

MEM MB DOS H0 D13
MEM MB DOS L0 C13
MEM MB DOS H1 A17
MEM MB DOS L1 B17
MEM MB DOS H2 B21
MEM MB DOS L2 C21
MEM MB DOS H3 D25
MEM MB DOS L3 C25
MEM MB DOS H4 AJ29
MEM MB DOS L4 AH29
MEM MB DOS H5 AK25
MEM MB DOS L5 AL25
MEM MB DOS H6 AJ20
MEM MB DOS L6 AJ21
MEM MB DOS H7 AL16
MEM MB DOS L7 AL17

MEM MB CLK H0 U30
MEM MB CLK L0 U29
MEM MB CLK H1 T29
MEM MB CLK L1 T28
MEM MB CLK L2 R31
MEM MB CLK L3 R30

MEM MB CKE0 J30

MEM MB CKE1 J28

MEM MB0_ODT0 AA30

MEM MB0_ODT1 AC30

MEM MB1_ODT0 AA31

MEM MB1_ODT1 AC29

MEM MB0_CS_L0 Y29

MEM MB0_CS_L1 AB29

MEM MB1_CS_L0 Y30

MEM MB1_CS_L1 AB31

MEM MB RAS_L W28

MEM MB CAS_L AA27

MEM MB WE_L AA28

MEM MB RESET# J27

MEM MB HOT# V28

MSI
MICRO-START INT'L CO.,LTD.

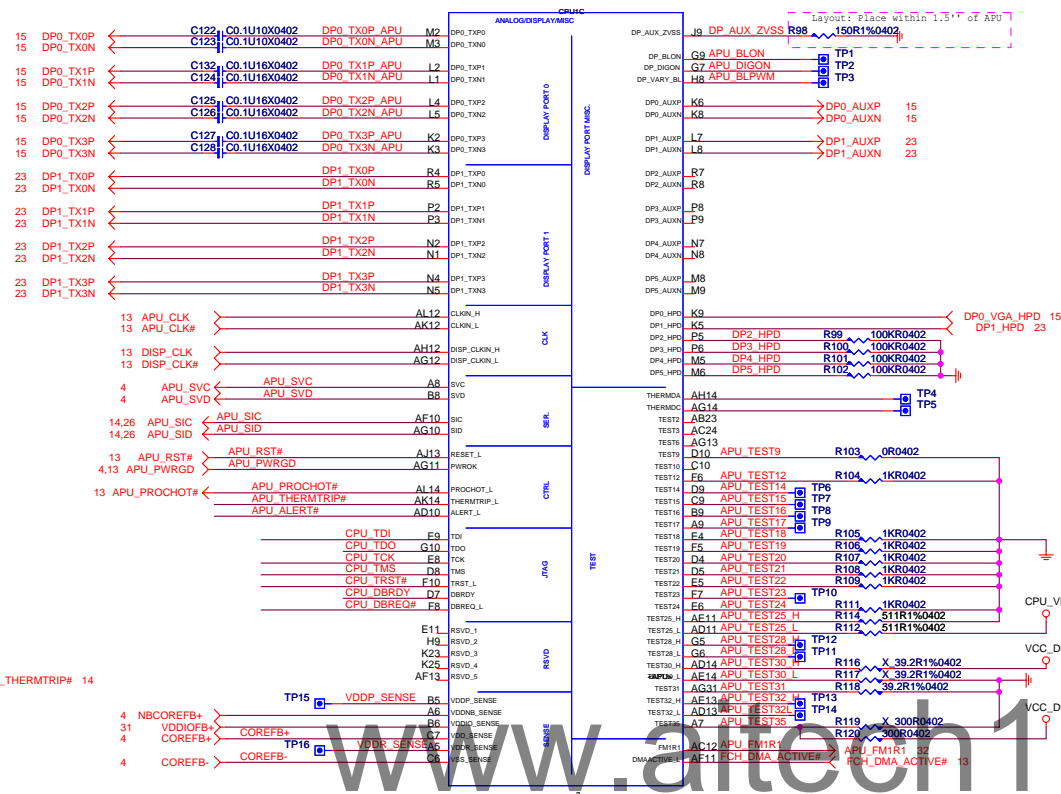
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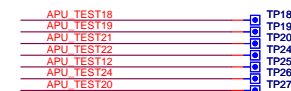
Date: Tuesday, May 17, 2011
Sheet: 7 of 37

Rev: **1.0**

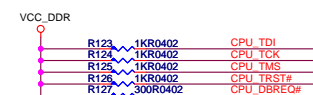
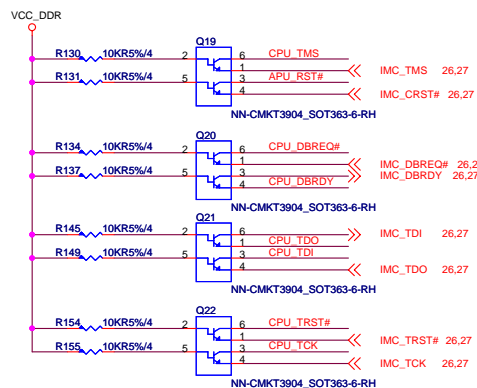
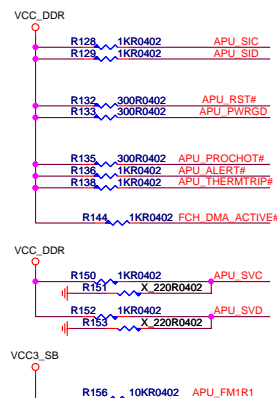
FM1 DISPLAY I/F



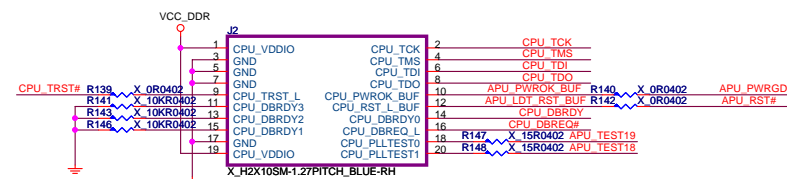
SCAN Connector

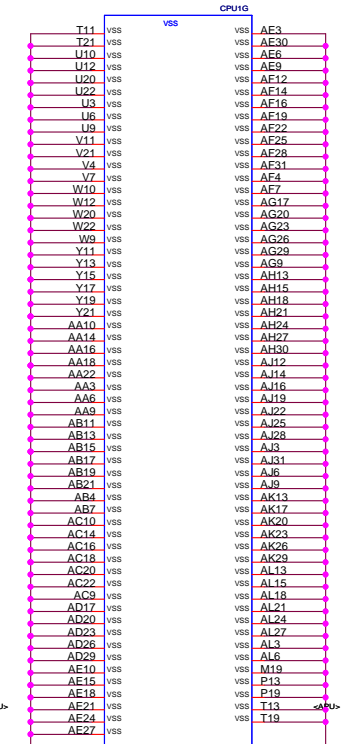
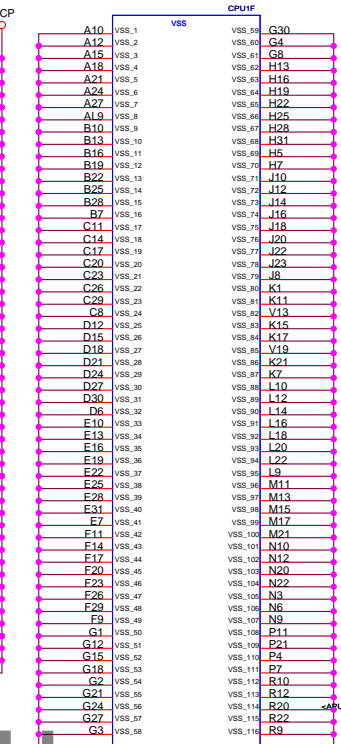
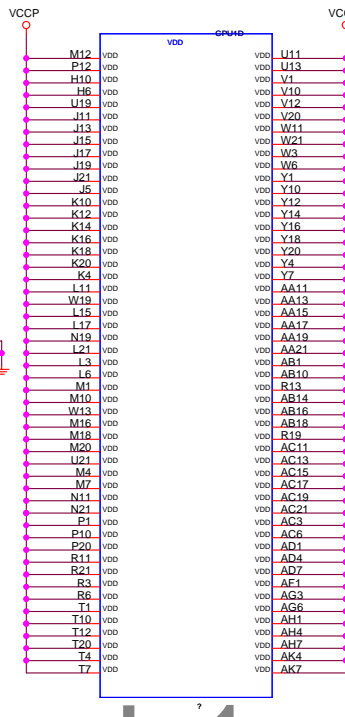
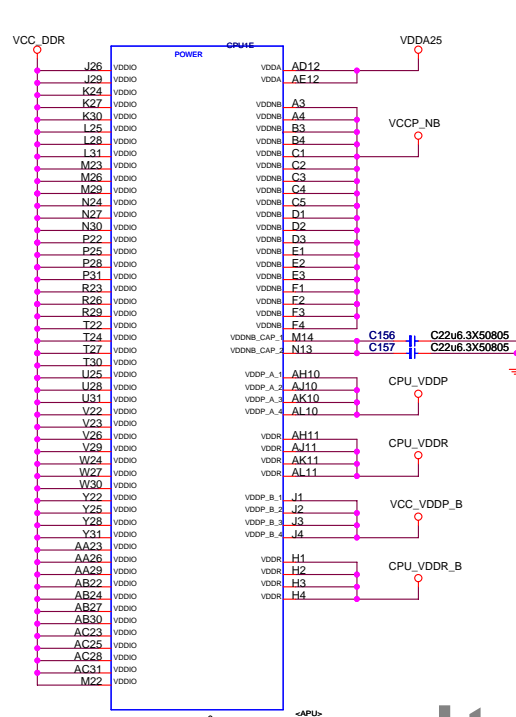
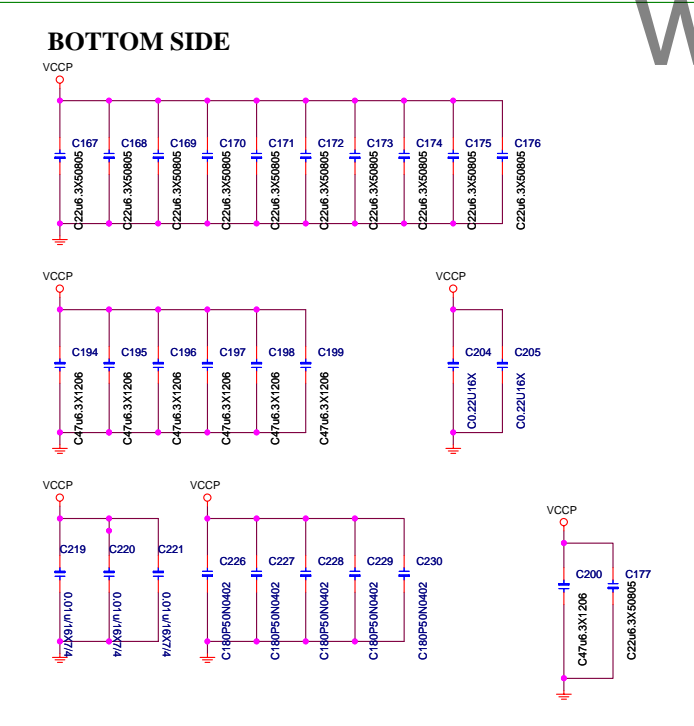
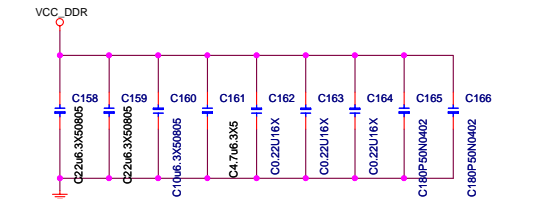
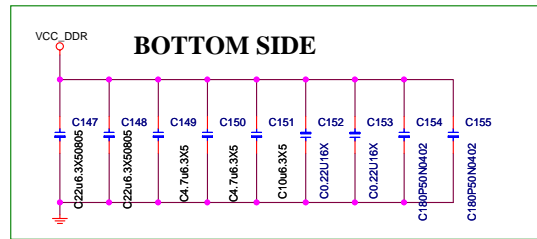
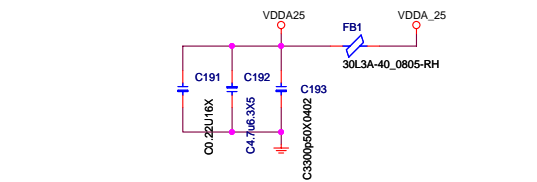


PULL UP



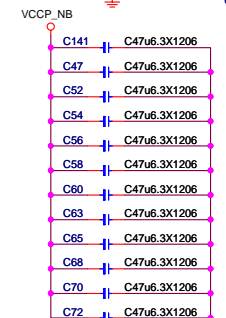
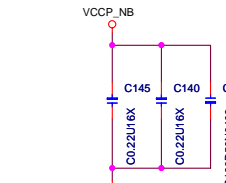
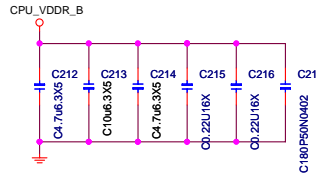
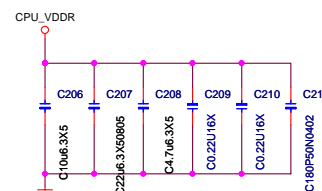
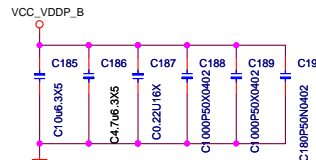
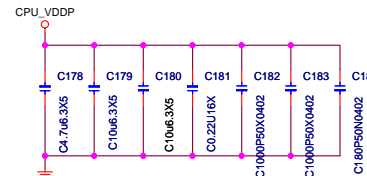
HDT+ Connector

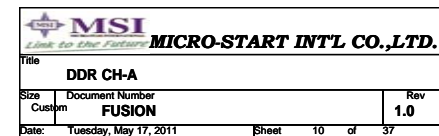


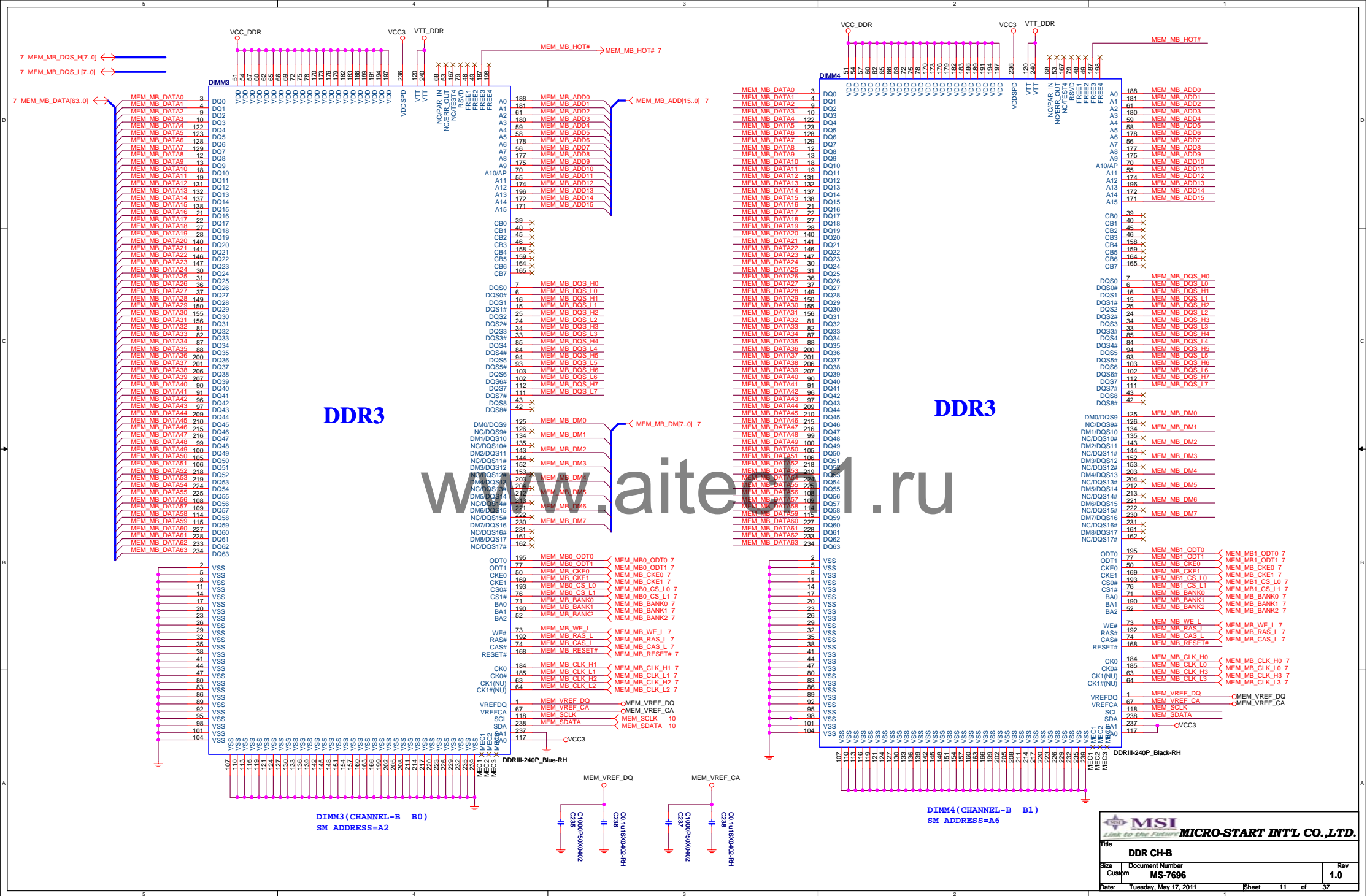


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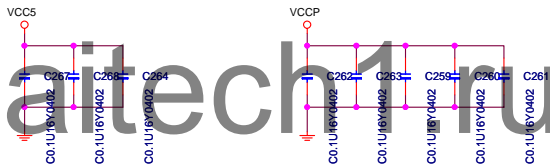
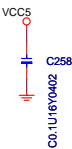
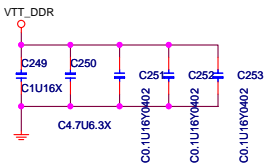
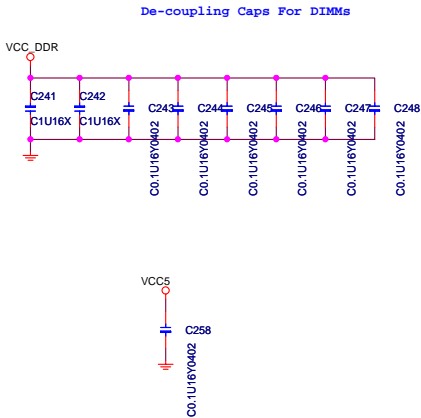
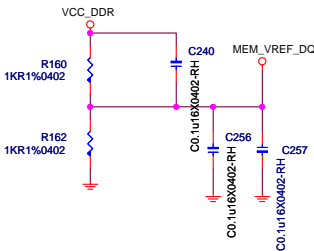
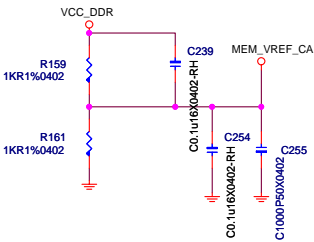
VDDP and VDDR support two separate power planes with single regulator



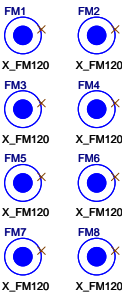




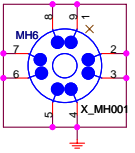
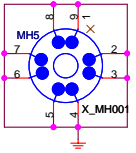
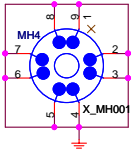
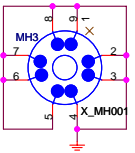
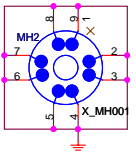
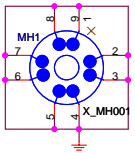
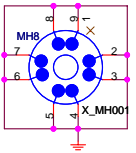
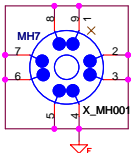
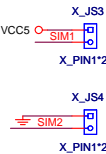
DDR REF POWER & CAPS



Optics Orientation Holes



Simulation

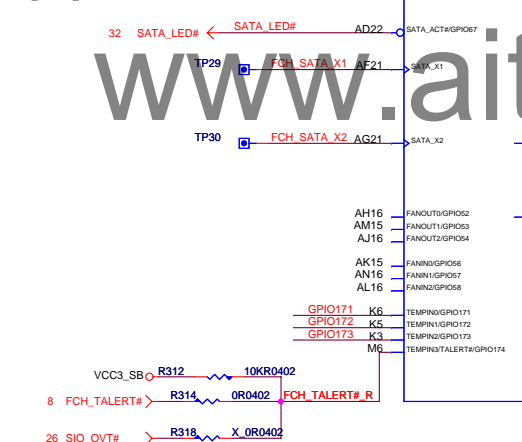
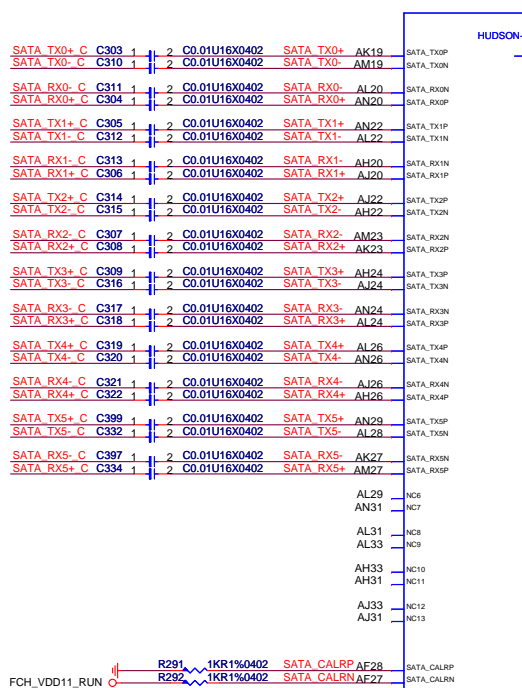
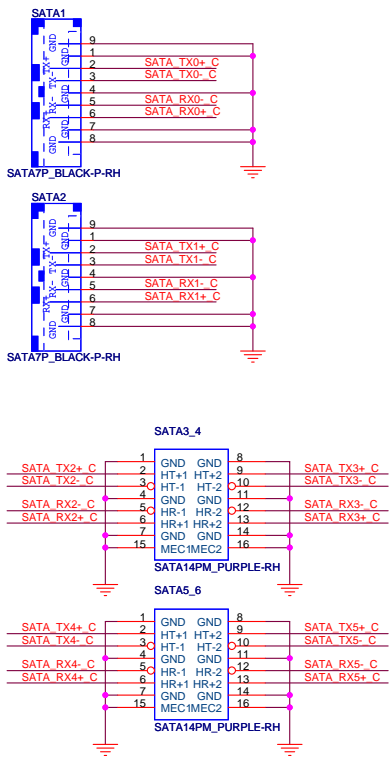


- VCCP CPU_VDD
- VCCP_NB CPU_VDDNB
- CPU_VDDR CPU_VDDR
- CPU_VDDP CPU_VDDP
- VDDA_25 CPU_VDDA
- VCC_DDR DDR_1V5
- VTT_DDR DDR_VTT
- VCC1P1 FCH_1V1
- +1.1VDUAL FCH_1V1_S
- VCC3_SB FCH_3V3_S
- VCC3_WAKE LAN_3V3
- VDD10 LAN_1V05

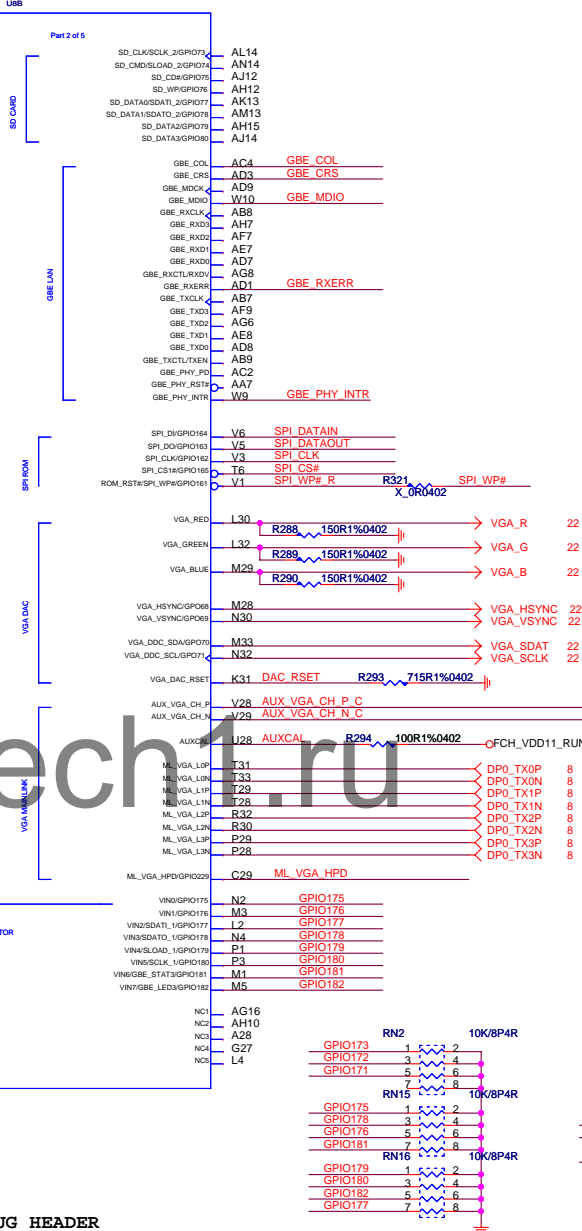
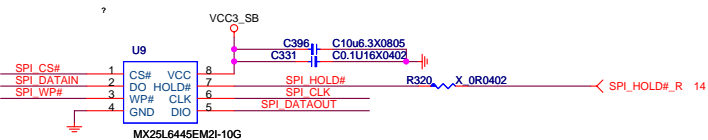
The diagram illustrates the internal circuitry of the S-RB751V-40 SOD323-RH component. It features a complex network of pins and internal components, including resistors, capacitors, and logic gates. The component is divided into several functional blocks:

- Power Domains:** S0 POWER DOMAIN (ROUTE TO DIMM, CLK Gen, SIO) and S5 POWER DOMAIN (ROUTE TO LAN, PCIe, PCI).
- I/O and Control:** Includes pins for SLP, FCH, and various control signals. It also shows the connection to a USB 3.0 port and a USB 2.0 port.
- Embedded Controller (EC):** The diagram shows the connection to the EC, which is responsible for power management and other control functions.
- USB:** The component includes a USB 3.0 port and a USB 2.0 port, both of which are connected to the internal circuitry.

The diagram is labeled 'HUDSON-2' and 'Part 4 of 5', indicating it is a multi-page schematic.

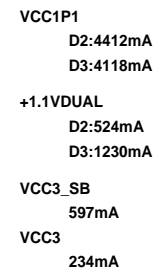


SPI ROM & DEBUG HEADER

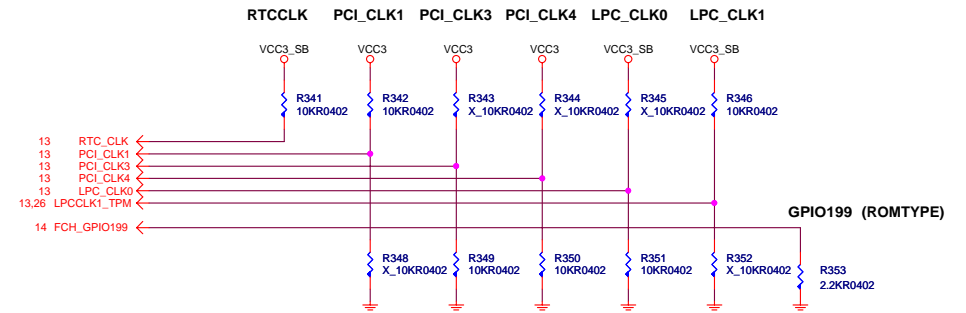


MSI
MICRO-START INT'L CO.,LTD.

Title			HUDSON SATA/VGA/SPI/HWM
Size	Document Number	Rev	
Custom	MS-7696	1.0	
Date:	Tuesday, May 17, 2011	Sheet	15 of 37



FCH REQUIRED STRAPS



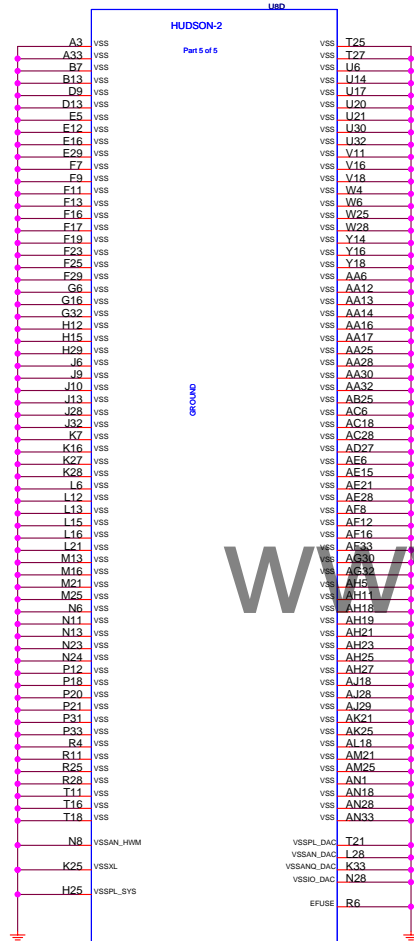
	RTCCLK	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO199 (ROMTYPE)
PULL HIGH	S5 Plus MODE DISABLED DEFAULT	PCIe interface at Gen2 DEFAULT	Enable Debug Straps	Reserved	EC ENABLED	Internal clock mode DEFAULT	LPC ROM
PULL LOW	S5 Plus MODE ENABLED	FORCE PCIe at Gen1	Disable Debug Straps DEFAULT	APU_CLK/DISP_CLK Required setting DEFAULT	EC DISABLED DEFAULT	External clock mode DEFAULT	SPI ROM DEFAULT

*This strap is not
used in External
clock mode

FCH DEBUG STRAPS

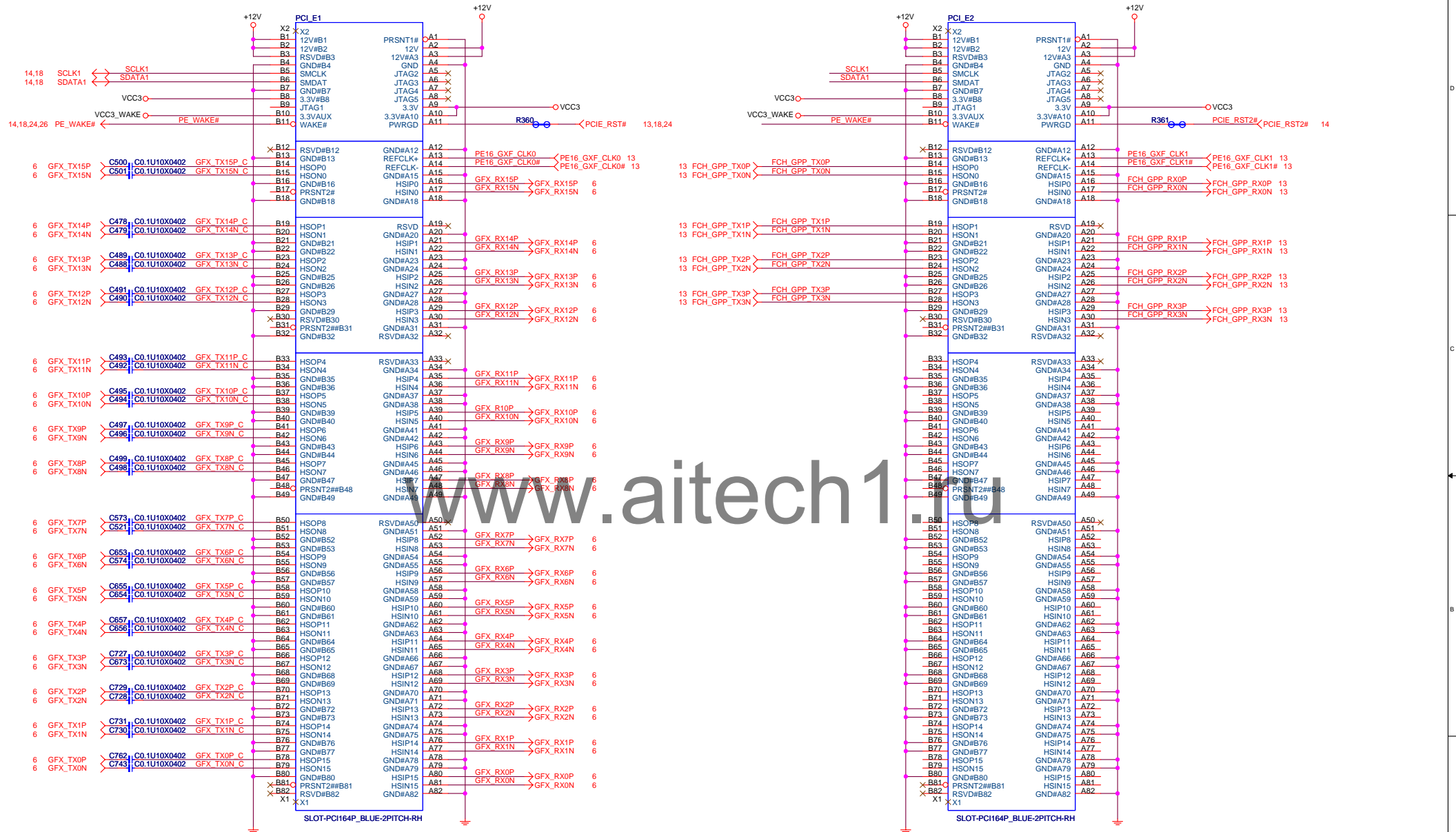


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	Use internal PLL clock DEFAULT			Disable I2C ROM DEFAULT	Use ROMTYPE straps DEFAULT
PULL DOWN	Bypass Internal PLL clock			Enable loading settings for UMI/PLL/misc from I2C ROM	Boot from PCI bus

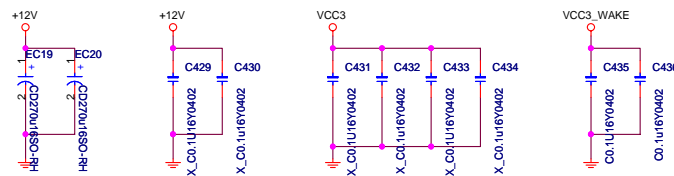


Layout:
VSSPL_SYS/VSSAN_HMM CONNECT TO GND
WITH A SEPARATED VIA

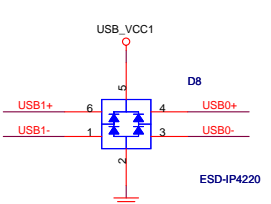
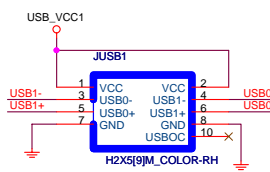
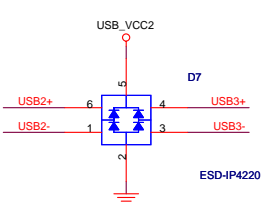
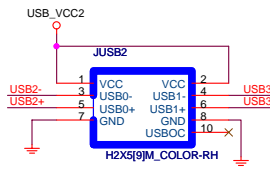
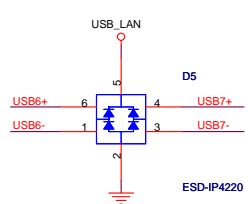
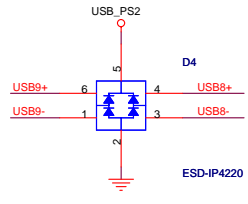
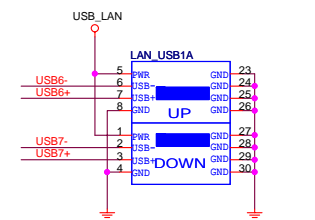
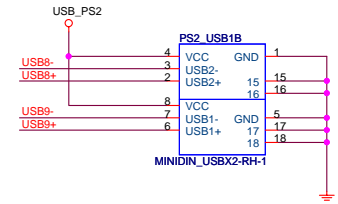
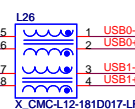
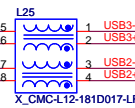
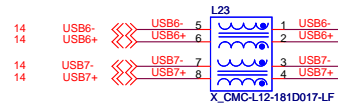
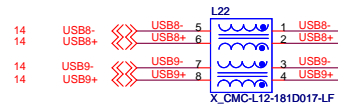
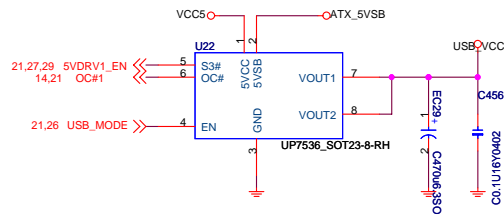
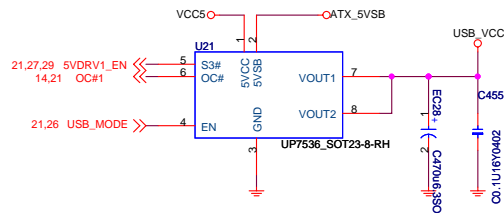
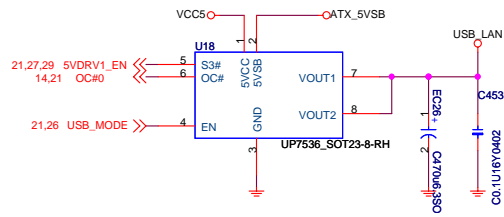
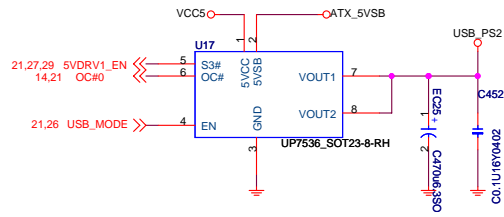
PCI EXPRESS x16 Slot



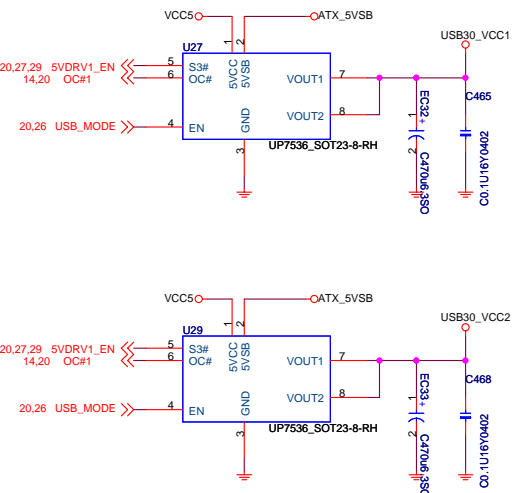
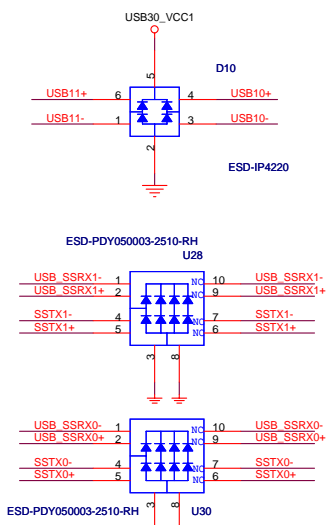
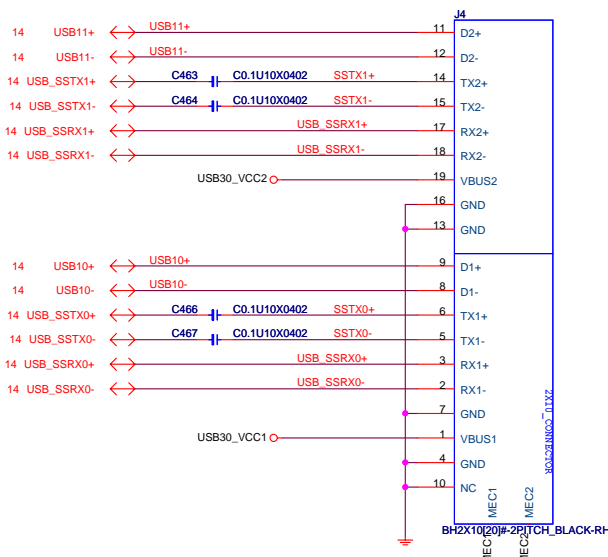
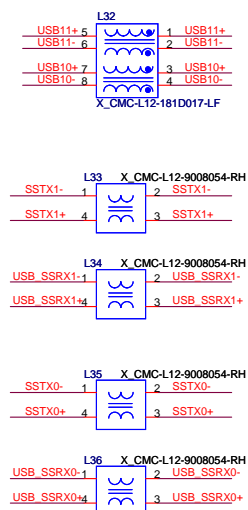
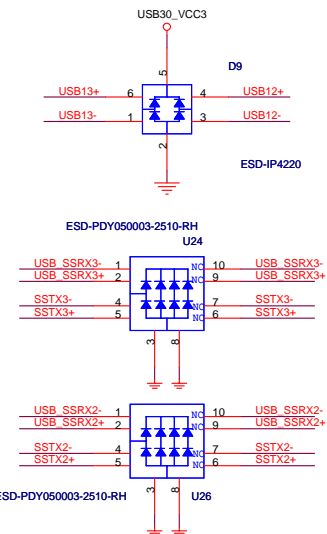
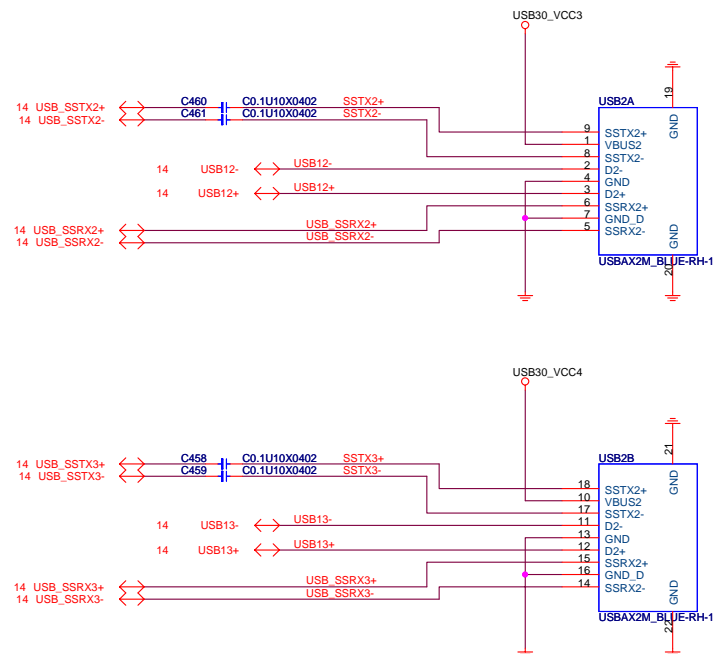
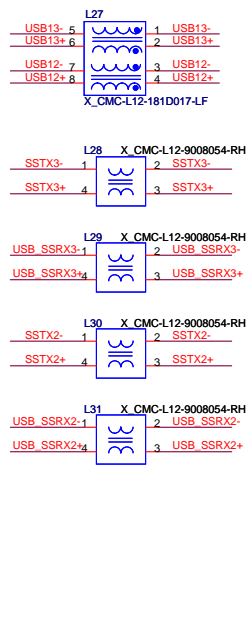
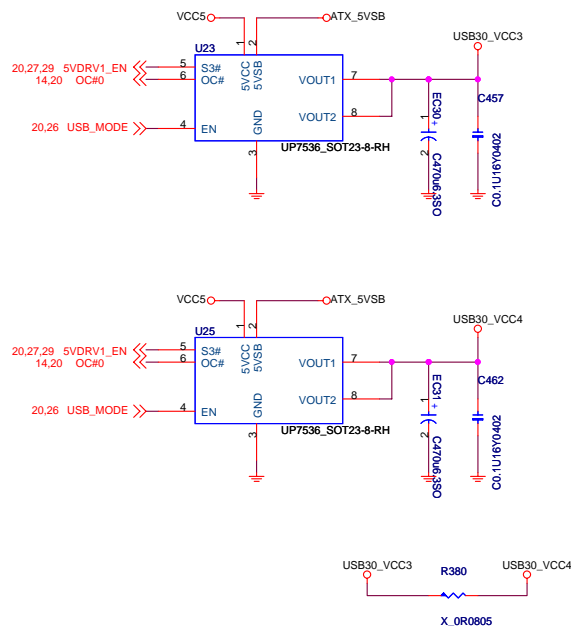
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POWER CIRCUIT FOR USB PORT 0,1

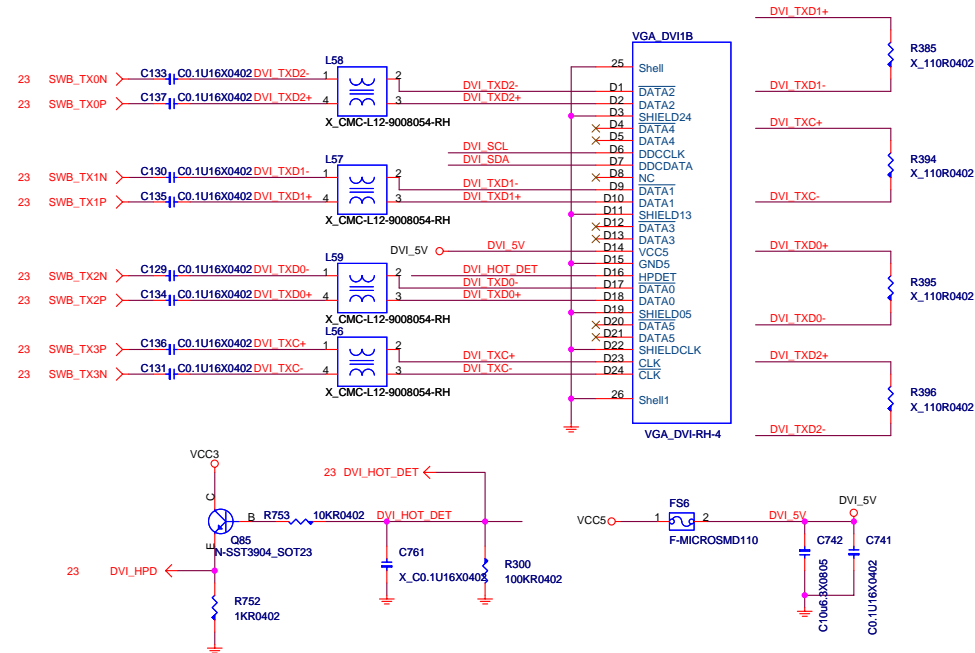


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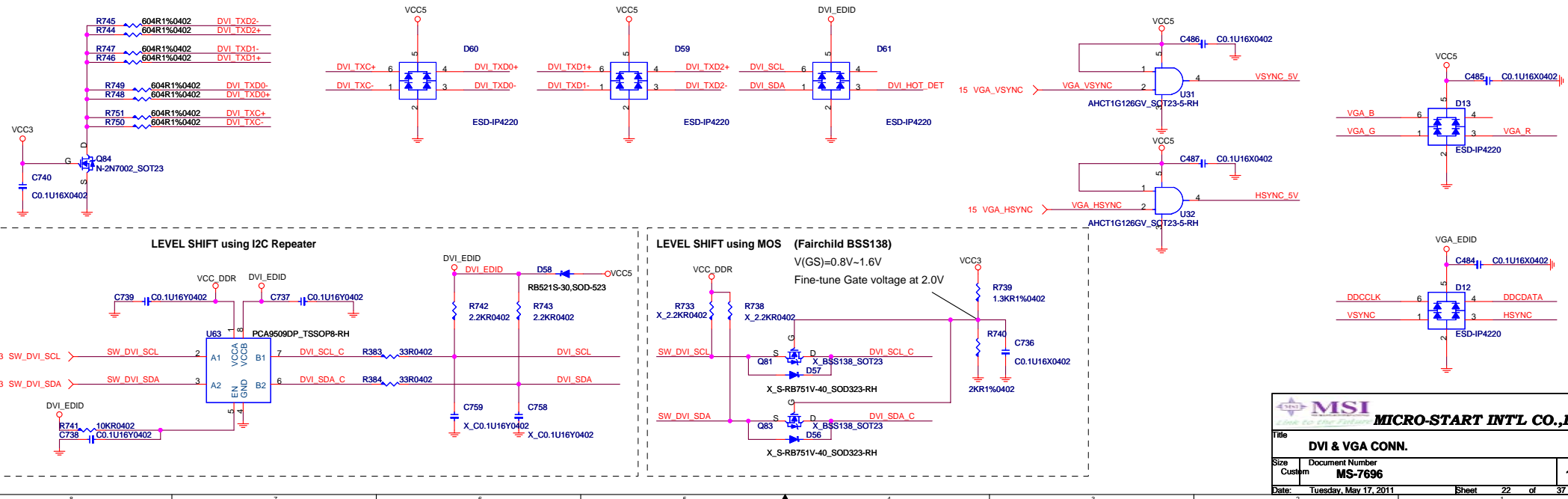
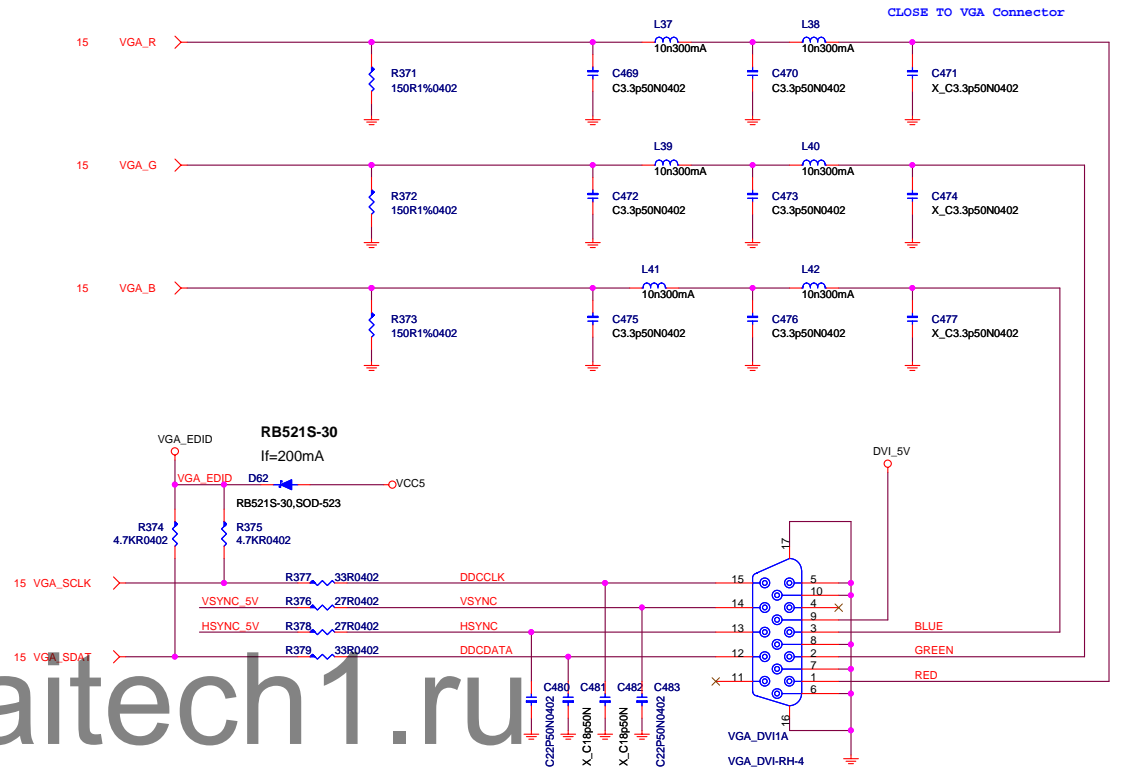


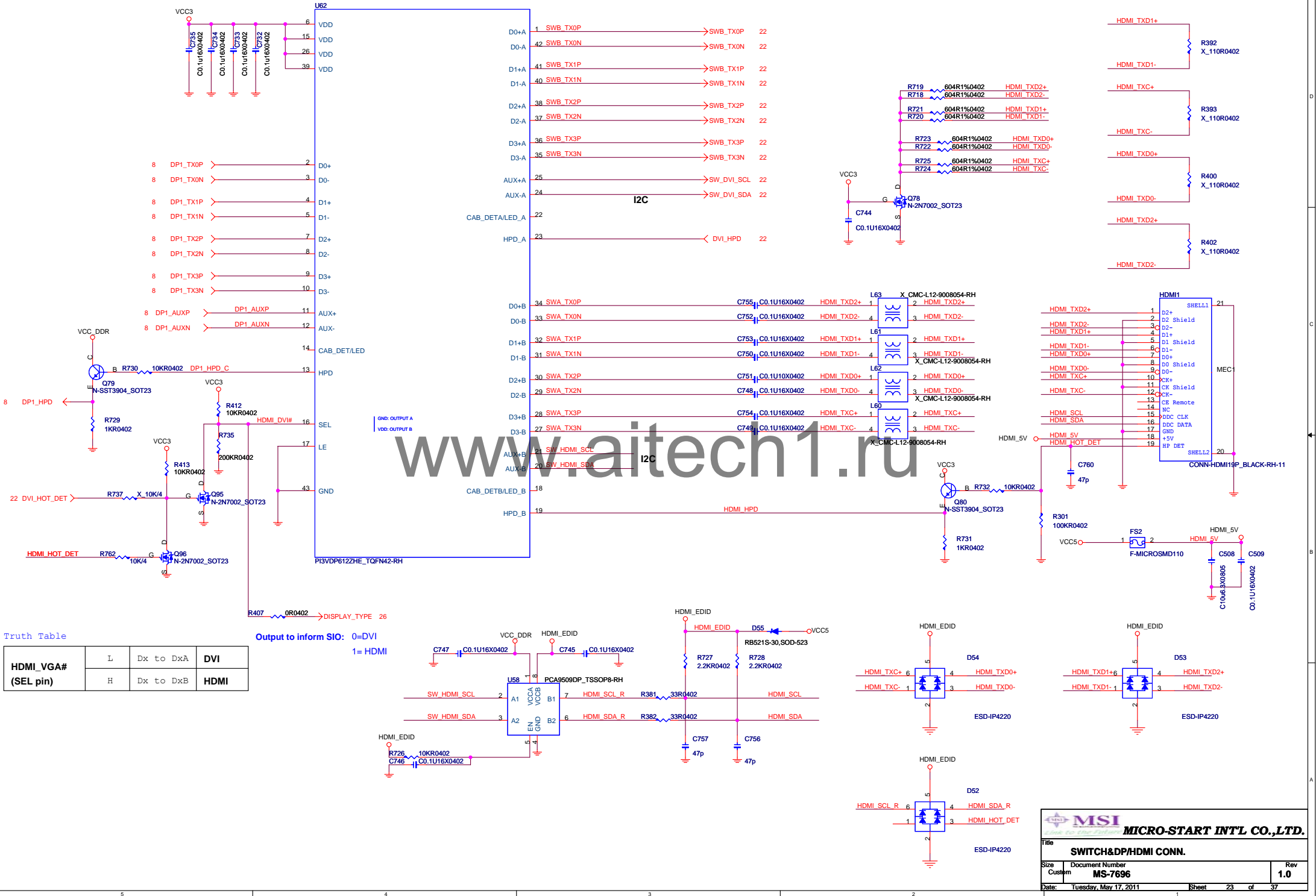
www.aitech1.ru

DVI CONNECTOR



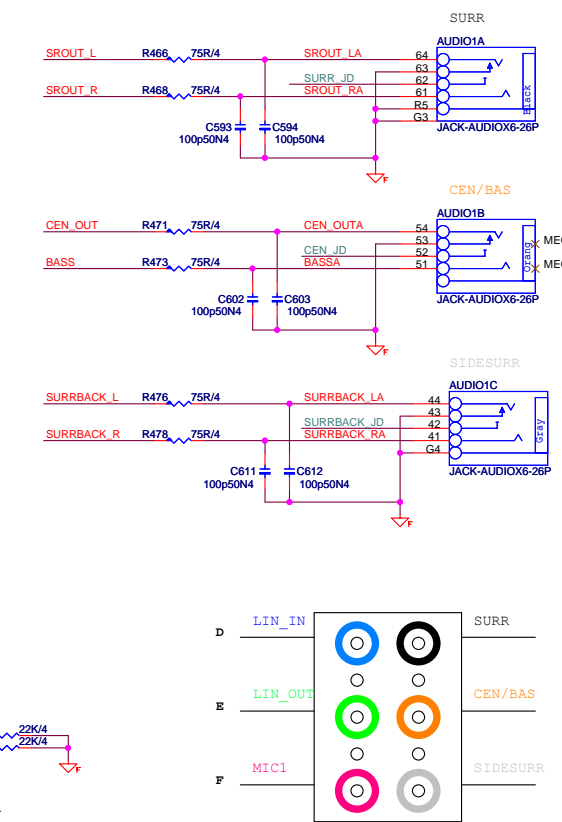
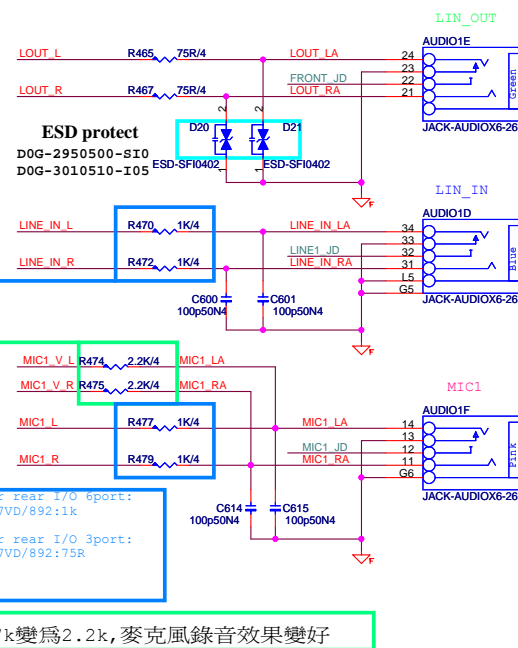
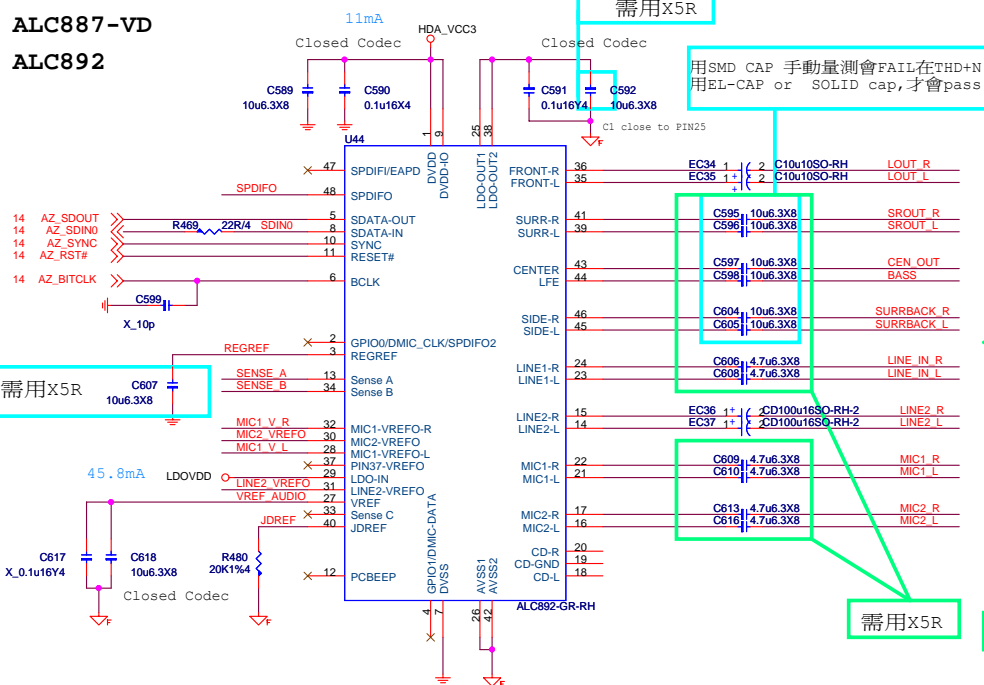
VGA CONNECTOR





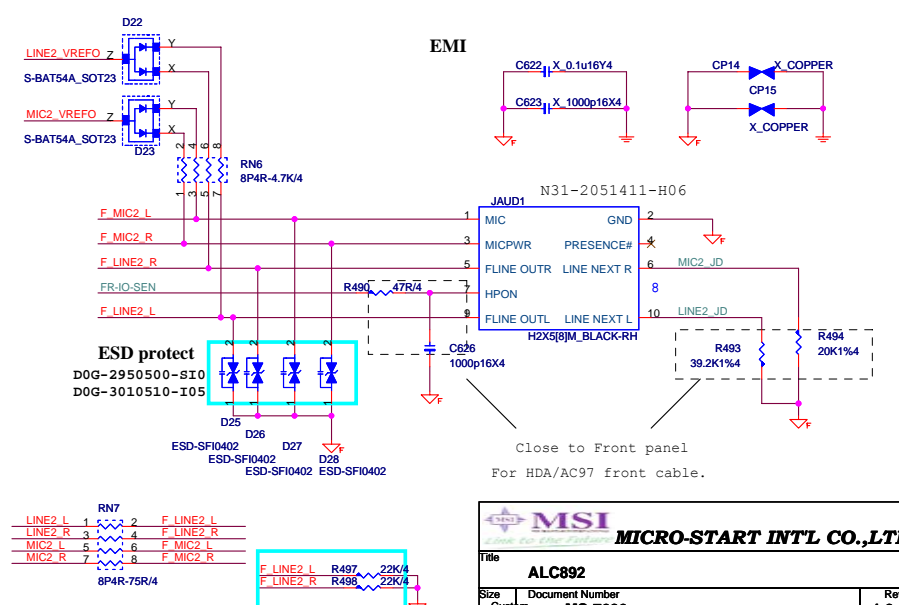
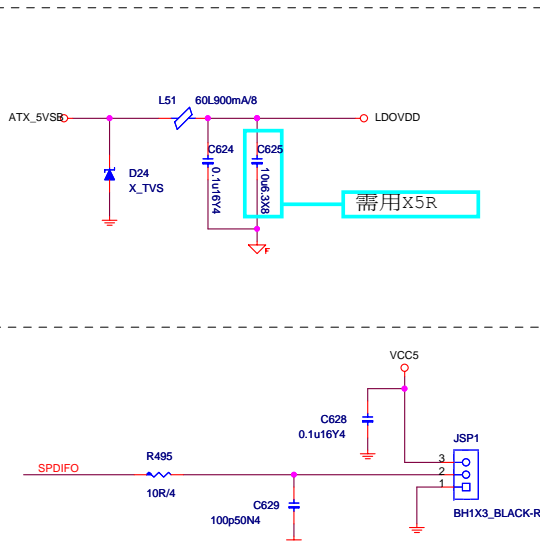
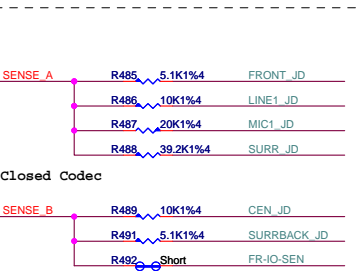
ALC887-VD

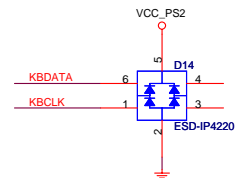
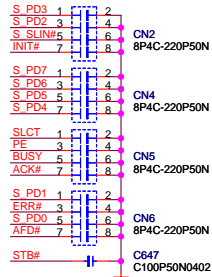
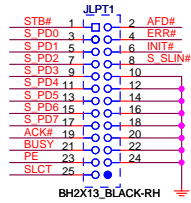
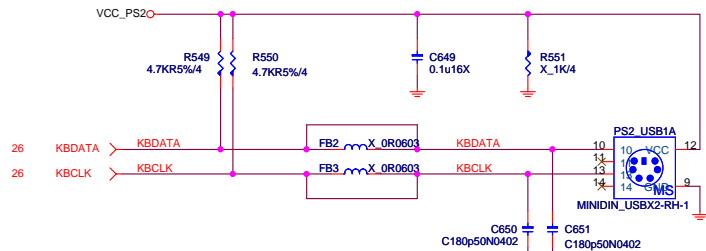
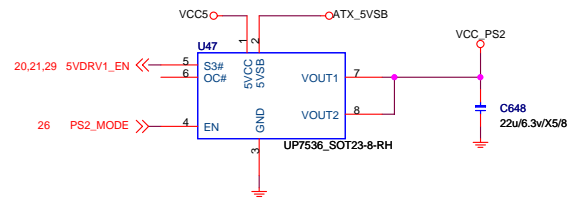
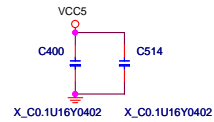
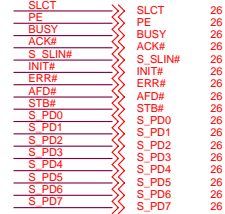
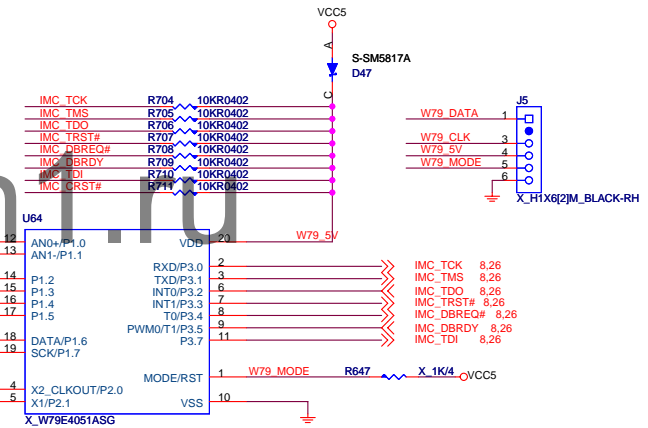
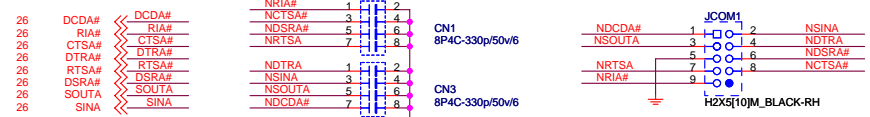
ALC892

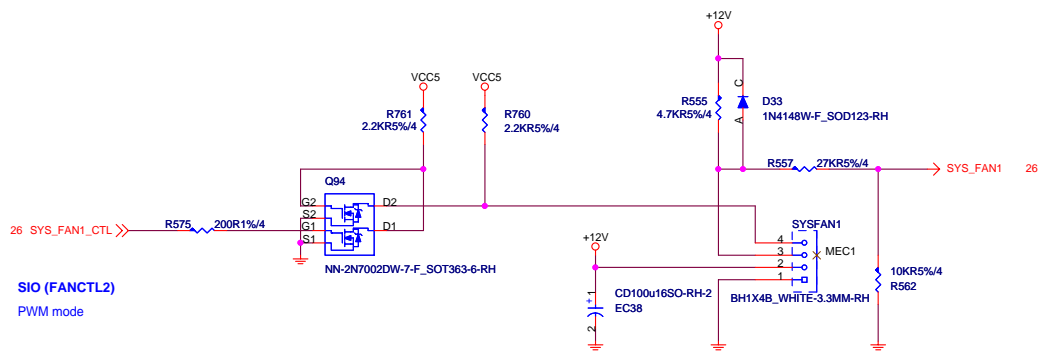


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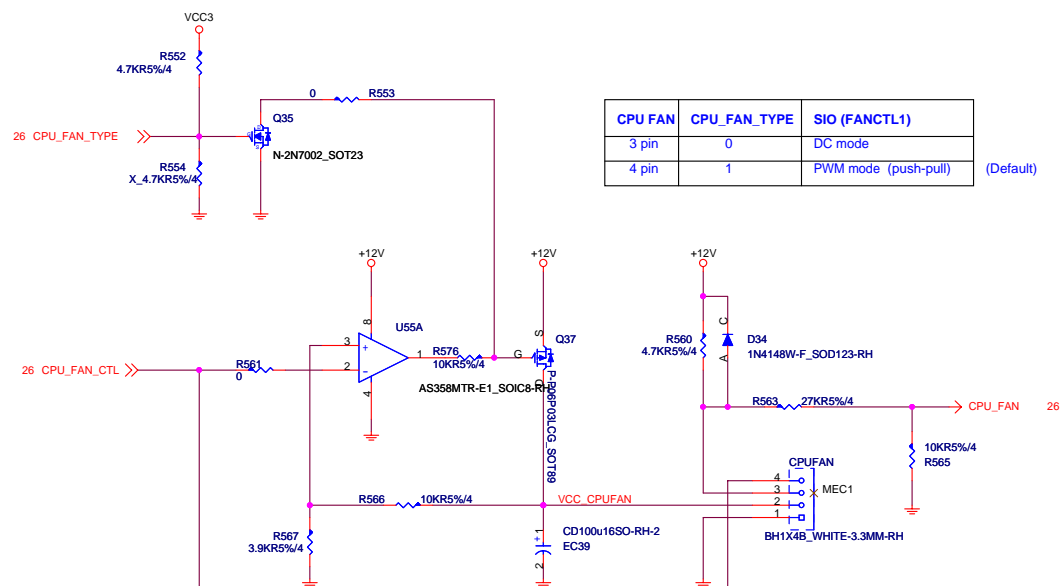
當串接電容有極性時，需上對地電阻



[illegible]

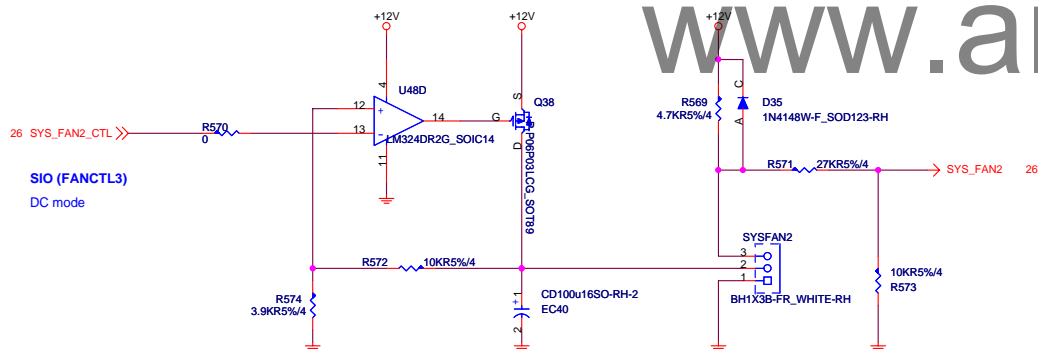


SIO (FANCTL2)
PWM mode



CPU_FAN	CPU_FAN_TYPE	SIO (FANCTL1)
3 pin	0	DC mode
4 pin	1	PWM mode (push-pull)

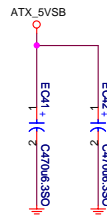
(Default)



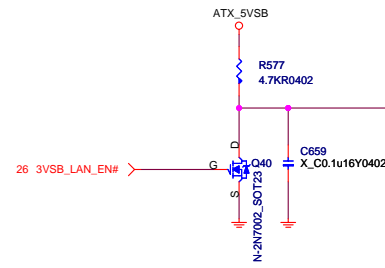
SIO (FANCTL3)
DC mode

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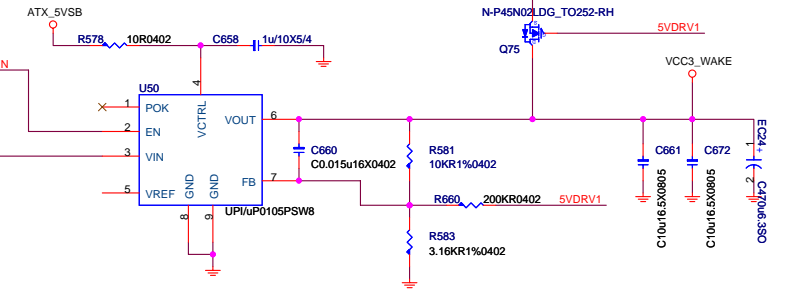
VCC5_SB Power Switch



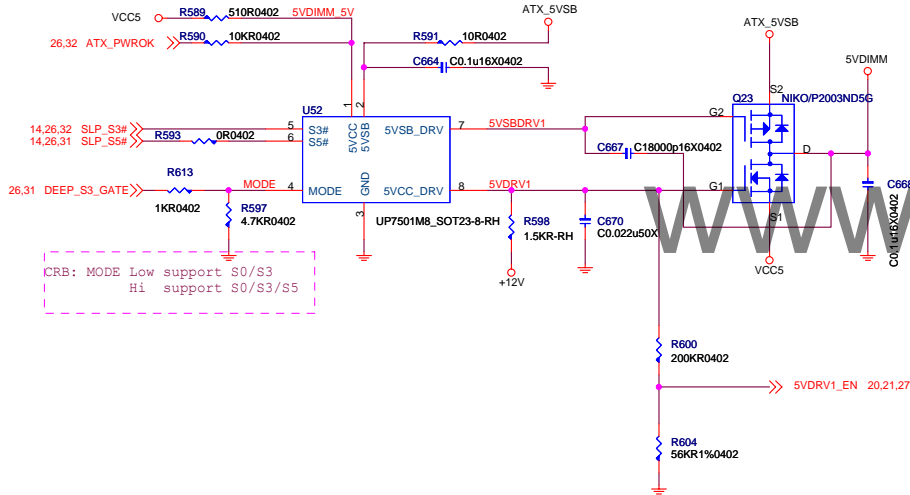
Trace Width 80mils.



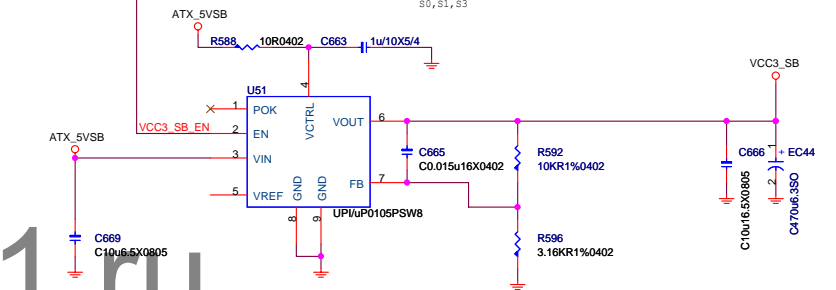
VCC3_WAKE POWER



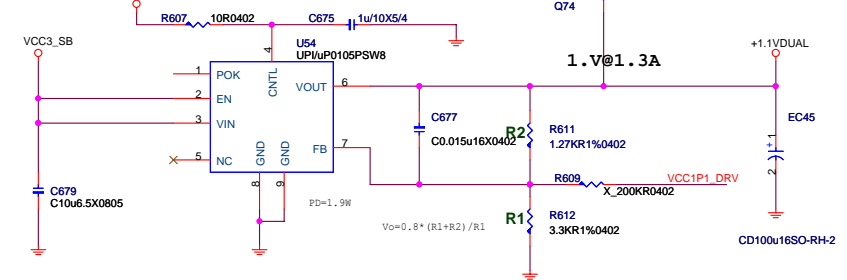
5VDIMM FOR DDR



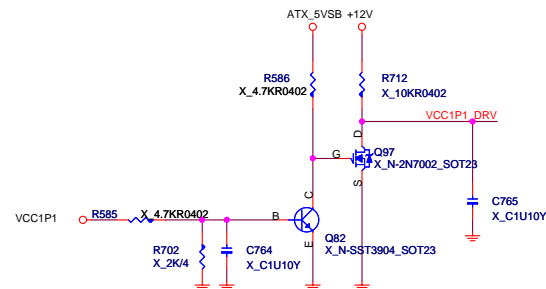
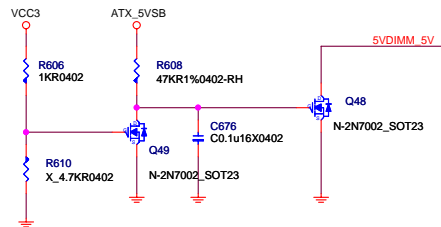
VCC3_SB POWER



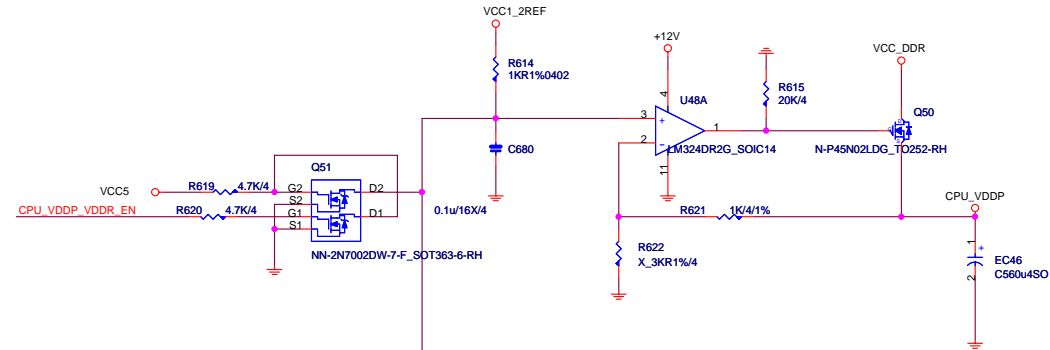
1.1VDUAL POWER



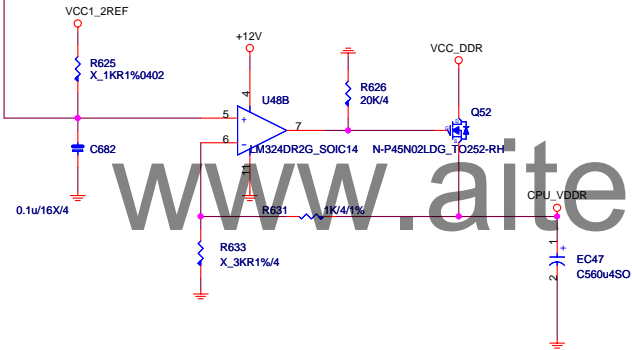
For special PSU sequence



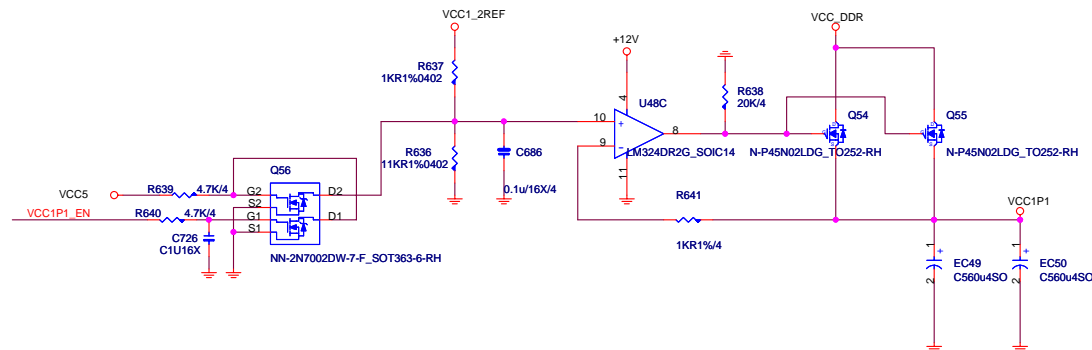
CPU VDDP POWER 1.2 V@3.5A



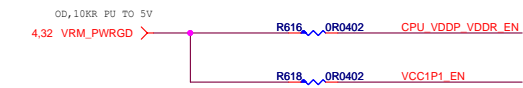
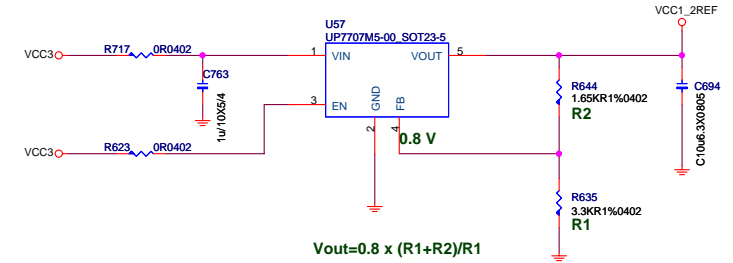
CPU VDDR POWER 1.2 V@4A



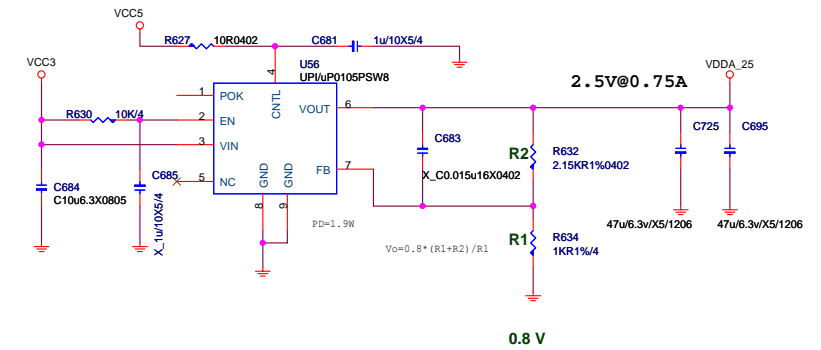
VCC1P1 POWER 1.1V@4.5A+1.3A



VCC1_2REF

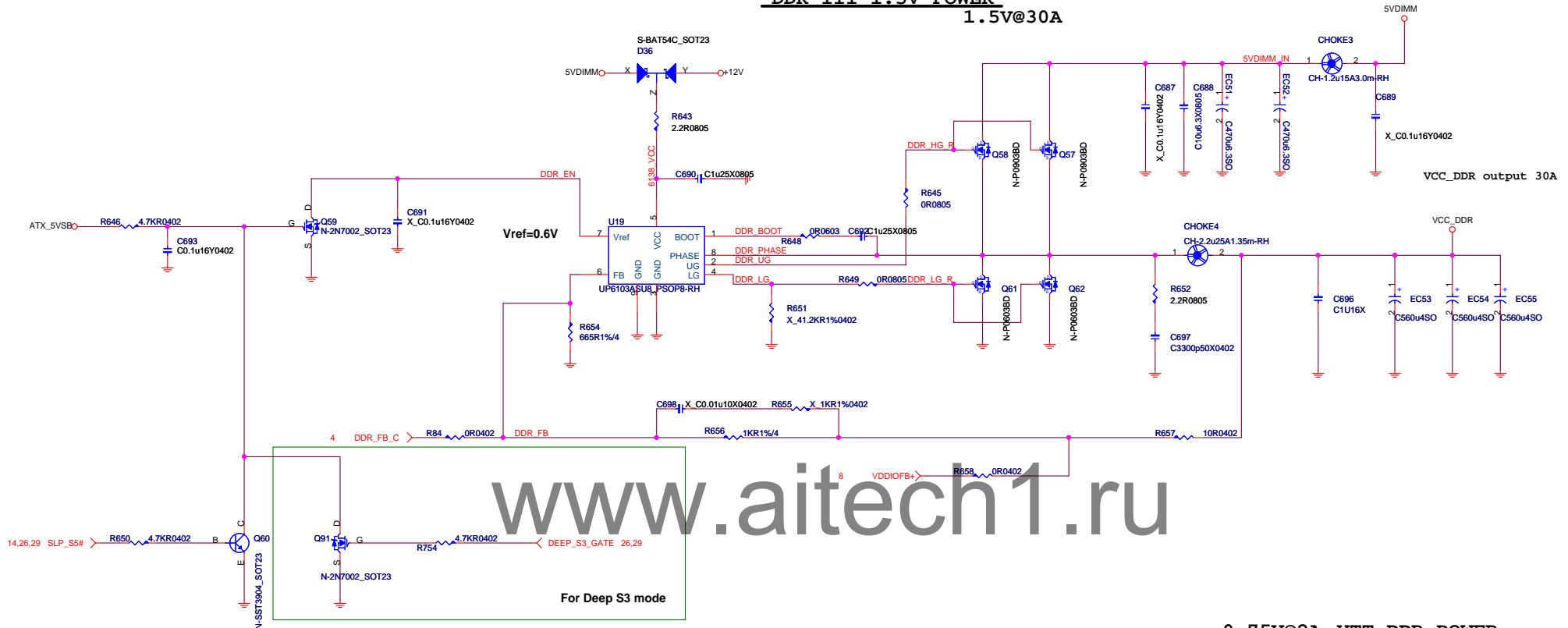


CPU VDDA_25 POWER

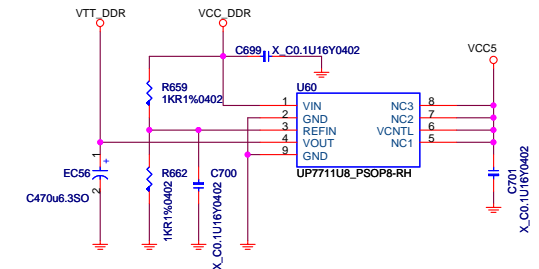


DDR III 1.5V POWER

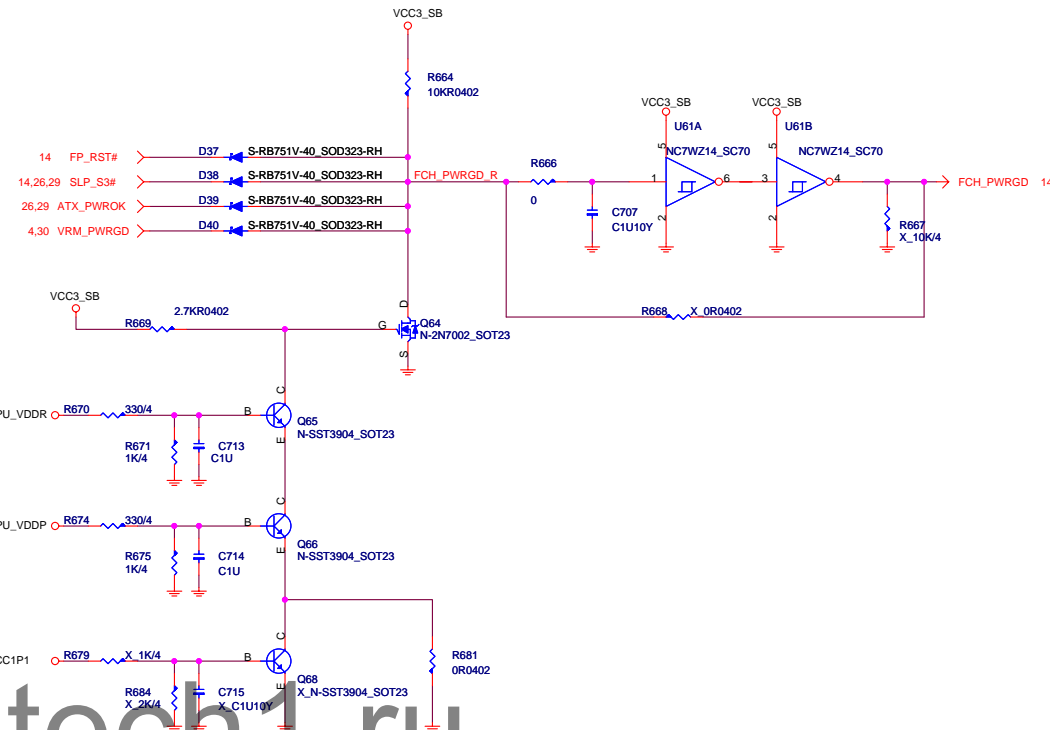
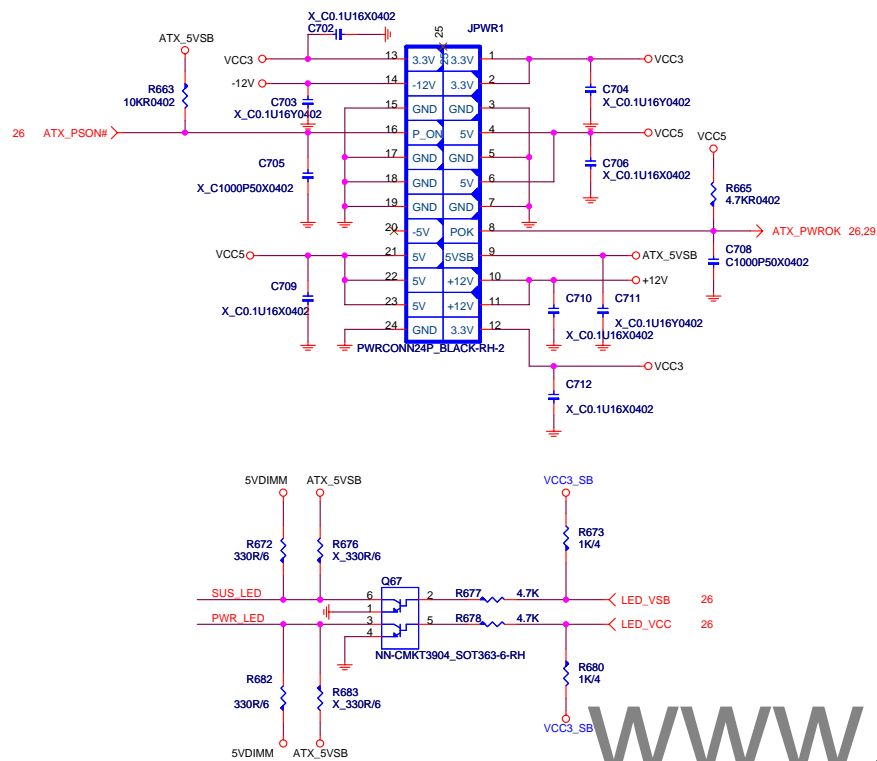
1.5V@30A



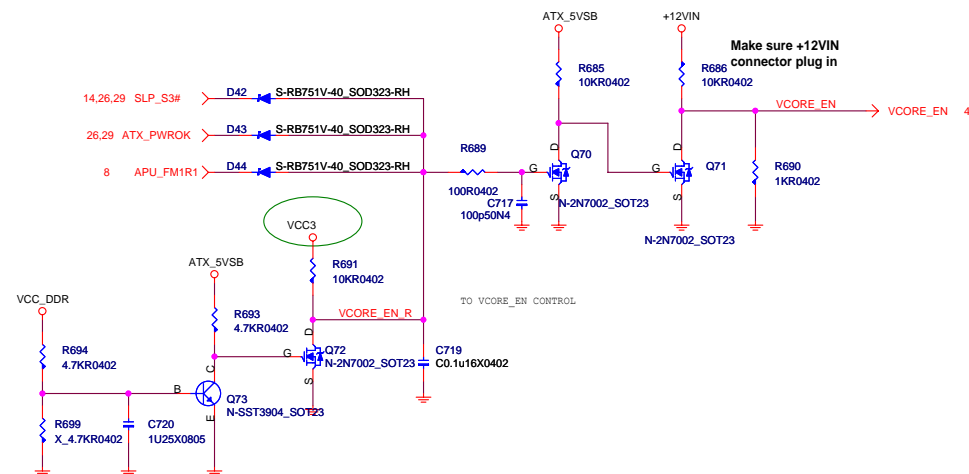
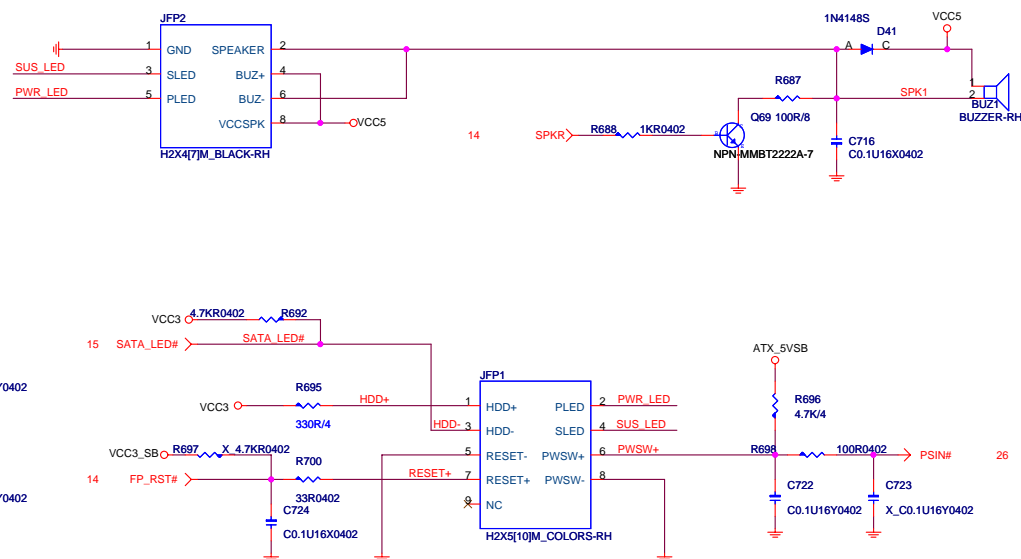
0.75V@2A VTT_DDR POWER



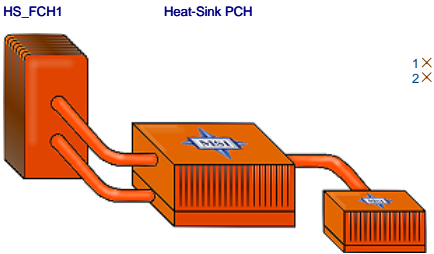
ATX CONNECTOR



BUZZER



HEAT SINK

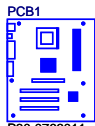


MANUAL PART



AVL:
D06-0100161-P52
D06-0100101-K26

BAT1_X1
BAT-CR2032-RH



PK0-0769610-G37
PK0-0769610-B48

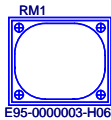
PCB1
P30-0763011



HDMI Royalty
HDMI




LABLE



RM1
E95-0000003-H06

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 MICRO-START INTL CO.,LTD.		
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0A-->1.0 modify list

Circuits

Page09 Add C200,C177

Page12 Add EMI CAP C264, C268, C267, C262, C260, C259, C263, C261

Page21 J4 pin10 tie to GND

Page26 Change MSDATA/MSCLK pull-up to ATX_5VSB

Page29 Reserve VCC1P1_DRV circuits

BOM

2011.05.11 Page04 Change R7,R12,C5,C8,R34,R28,R27,C17,C18,C20 value for AMD spec
Change CHOKE1 to L04-12A7321-L65 for costdown
Change U1 to I32-6328C2C-I11

Page09 Add C200,C177 for AMD spec

Page12 Add EMI CAP C264, C268, C267, C262, C260, C259, C263, C261


Page25 Change EC34,EC35 to C71-1001020-N07

Page29 Delete Q74, R609

Page31 Delete C691
Change CHOKE1 to L04-12A7321-L65 for costdown

2011.05.13 Page04 Change R28,R27,R54,C19,C20 value for AMD spec

2011.05.17 Page04 Change R27,R54 value for AMD spec

 MICRO-START INTL CO.,LTD.		
Title		
History		
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